Products and Technologies for Advanced Wafer Processing

Drive Innovation, Deliver Excellence

ASM International
Analyst and Investor Technology Seminar
Semicon West  July 11 2012
• **ASM Front-end Products and selected applications**
  - ALD High-k gate/metal gate
  - PEALD for Spacer Defined Double Patterning
  - Epitaxy
  - Low-k
  - Vertical Furnace

• **Platform roadmap**

• **Summary**
Scaling will increasingly be enabled by New Materials and 3D Technologies


Scaling enabled by Litho

Scaling enabled by Materials

Scaling enabled by 3D

Low-k

Strained Si

High-k

FinFET

3D SIC

3D Memory

IEDM 2002

IEDM 2003

SiGe

IEDM 2007

Chipworks 2012
### Market Requirements: 32nm → 22nm → 14nm and beyond

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**Strong IP protected portfolio**
# ASM Products – Front-end

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**Strong IP protected portfolio**
High-k Metal Gate: Gate Dielectric

- Current practice: Hf based (HfO₂ or HfSiO₄) from HfCl₄/SiCl₄/H₂O
  - So far, MO chemistries have proven to be inferior (roughness, leakage, reliability)
- Migration towards HfO₂ as the standard because lower Equivalent Oxide Thicknesses (EOT) can be reached
  - EOT’s in the range of 0.7-1.2nm demonstrated with HfO₂
High-k Material Adoption Trend
High Performance and Low Standby Power

- ALD HfO$_2$ is the only material for HP devices
- High-k for LSTP devices will transition to ALD HfO$_2$
- Convergence to gate last process for all logic to enable optimization of work function
Transition to 3D Fully Depleted Devices and the Importance of Conformality

- Metal and high-k over very challenging topography
- EOT and work function have to be uniform over fin height
- FinFET’s drive need for conformal films with uniform thickness, composition and micro-structure
Perpendicular to Fin

- Metal and high-k over very challenging topography
- EOT and work function have to be uniform over fin height
- Success of FinFETs is enabled with ALD metal gates
- Entire spectrum of work functions researched and available from ASM
• ALD HfO$_2$ has become the de-facto high-k standard
• Gate last process will be used for logic to enable work function optimization of the metal gate electrodes
• 3D FinFET’s drive adoption of ALD, not only for the dielectric, but now also for metals
• Metals and damascene like process flows have penetrated the Front-end of the Line
• **Pulsar® XP**
  • ALD for high-k
  • Cross-flow reactor
  • Solid source delivery system

• **EmerALD® XP**
  • ALD for metal gates
  • Showerhead reactor
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**Strong IP protected portfolio**
Spacer Defined Double Patterning

- After PEALD SiO₂ deposition (on full stack)
  - PR/BARC
  - PEALD SiO₂
  - SiOC
  - a-C
  - Polysilicon
  - Si substrate

- After PEALD spacer etch-back and photoresist strip
  - PEALD spacer

- After SiOC opening
  - SiOC

- After a-C opening
  - SiOC
  - a-C

- After polysilicon etching, without a-C removal
  - Poly-Si

- After polysilicon etching, with a-C removal
  - Poly-Si
• **Spacer defined quadruple patterning**: two sequences of spacer pattern transfer
• **MIR 3000**
  
  - PEALD of SiO$_2$ for Spacer Defined Double Patterning
  
  - High productivity XP cluster with 2 PEALD modules, each processing 4 wafers
  
  - PEALD enables tunable SiO$_2$ film properties, to optimize for film quality or ease of film removal
### ASM Products – Front-end

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Extendibility of ASM’s Low-k Solution

- HVM since 2001
- Aurora®Lowk
- Aurora®ULK
- Visibility until 2017
- Aurora®ELK(UV)
- UV assisted Porogen
Introduced during Semicon West 2012

- **XP8**
  - High productivity single wafer tool for both PEALD and PECVD applications
  - Accommodates up to 8 chambers for PEALD or PECVD
  - PEALD and PECVD can be integrated on the same platform
### Market Requirements: 32nm → 22nm → 14nm and beyond

#### Process
- **ALD and PEALD**
  - ALD solution (Hafnium oxide)
  - PEALD Low temp dielectrics

#### Application
- **ALD** key for High-k Metal Gate technology
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#### ASM Relative Positioning
- #1 in the served ALD market
- Qualified by nearly all Logic manufacturers
- Strengthening inroads into Memory with PEALD

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**Strong IP protected portfolio**
• Number of epi layers dependent upon the breakdown voltage required (i.e. product application specific)
• Typical breakdown voltages from 600 – 800V
• Implemented in production by various companies

**ASM Product: Epsilon® 3200**
Epi for advanced power devices
ASM Front-end Products
Epitaxy

Introduced during Semicon West 2012

- **Intrepid® XP**
  - Epi for advanced CMOS strain
  - High productivity system using ASM’s XP cluster with 4 Epi reactors
  - Integrated Pre-Clean for pre-Epi interface control
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A412 PLUS: Productivity and Innovation

Productivity
- One A412 PLUS = up to 80 kwpm (2.5 hr process, 95% available, 150 wafer boat)
- About 40% lower capex per m² as competitors
- Dual boat/dual reactor system

Real time production data:

![Graph showing Wafers Out in one Day over 24 hrs from 04/11 0:00 to 04/12 0:00]

Innovation
- Addition of ALD processes
- Example: Batch ALD TiN process

![SEM images showing film thicknesses: 57.7 nm, 56.1 nm, 55.0 nm, and 56.1 nm at TOP, CENTER, and BOTTOM]
Wafer Fab Equipment Forecast

Share of 28nm, 22nm and 14nm of total Equipment spending increasing in 2012-2013

Key customer ALD penetrations in 28 and 22nm: market segments with high expected growth

Gartner June, 2012
Summary

- Adoption of more ALD and PEALD applications in HVM continues
  - #1 position in ALD for High-k gate
  - 3D FinFET’s drive adoption of ALD, not only for the dielectric, but also for metals
  - strong inroads into patterning applications with PEALD
- Introduced Intrepid® XP, system with 4 Epi reactors, for CMOS strain Epi
- Introduced XP8, high productivity system for PEALD and PECVD applications
- ASM’s Vertical Furnace is providing the lowest CoO and footprint per reactor
- 450mm development started and first tools have been shipped

Drive Innovation, Deliver Excellence