New Materials as an enabler for Advanced Chip Manufacturing

Drive Innovation, Deliver Excellence

ASM International
Analyst and Investor Technology Technology Seminar
Semicon West July 10 2013
• New Materials: Moore’s Law Enablers
• Major Trends in Thin Film Deposition
  • The ALD Technology Platform as a Response
  • FinFET related challenges and Metal ALD
  • PEALD as a Low Temperature Enabler
• ASM Front-end Products and selected applications
• Summary and Conclusions
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Scaling will increasingly be enabled by New Materials and 3D Technologies


Scaling enabled by Litho

Scaling enabled by Materials

Scaling enabled by 3D

Low-k

Strained Si

High-k

FinFET

3D SIC

3D Memory

IEDM 2002

IEDM 2003

SiGe

IEDM 2007

Chipworks 2012
New Materials and Processes: Moore’s Law Enablers

**Higher Capacitance, Lower Leakage**
- High-k and Metal Gates
- DRAM, RF, decoupling capacitors

**Higher Mobility, Lower Resistance**
- Strain and new Channel Materials
- New metal contacts

**Less Cross Talk, Faster Interconnect**
- (Porous) Low-k Materials
- Improved Metals

**Smaller Feature Sizes**
- Sub-Rayleigh limit patterning using SDDP
- Anisotropic Etch
- Conformal SiO₂
- Pitch/2
ALD enables new materials and 3D

• New materials and 3D applications require more precise and controlled thin film deposition

• Compared to conventional deposition techniques ALD offers superior:
  • Uniformity
  • Conformality
  • Interface control

• **ASMI is a leading player in the ALD market**
  • Developing ALD technology since 1999
  • Strong IP position
  • Number 1 in high-k gate and strong position in SDDP

• **The ALD market offers strong growth opportunities:**
  • High-k metal gate, FinFET
  • Spacer defined double patterning
  • Other emerging applications
What is Atomic Layer Deposition (ALD)?

Step 1: (Metal) Precursor Chemisorption

Step 2: Purge

Step 3: Reaction to Oxide/Nitride with O₂, H₂O, NH₃ co-reactant

Step 4: Purge

and repeat…
Key strengths of ALD relative to conventional deposition

**Uniformity**

- Mean: 291.0133
- Maximum: 292.6831
- Minimum: 288.7532
- Std. Dev: 0.9647908
- Range: 3.9299
- HI/Lo Var: 0.66%

29 nm SiO₂ <1% 3σ <0.7% M-m

**Step Coverage**

SEM's Courtesy of Philips Research Labs

**Interface Control**

Atomically engineered interfaces to optimize leakage current, reliability and work-functions

20 nm

**Composition Control**

Excellent composition control for ternary alloys such as GST and STO

V. Pore (2010)
ASM’s unique Materials Development Capabilities

**ASM Microchemistry (Fi)**
Pre-cursor Exploration
Process Feasibility
Basic Materials R&D
Cooperative R&D Projects

N+\geq3

**ASM Belgium**
Process Development
Process Integration 15 – 7 nm
Cooperative R&D Projects

N+2,3

**ASM Europe**, **ASM America**, **ASM Japan**, **ASMGK (Korea)**
Product Development, Product Engineering, Product Marketing, Cooperative R&D Projects

N+1,2
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Major Trends in Thin Film Deposition and ASM’s Vision for ALD

Thin Film Needs:
- New materials
- Thinner films
- Interface engineering
- 3D conformality
- Lower thermal budget

Integration Capabilities
- Subtractive and Damascene patterning
- Etching
- Gap fills
- Clustering

ALD is a whole new technology platform for enabling new materials!

ALD → PEALD → ....
FinFET Challenges: ALD enables Further Scaling in 3D

- Materials properties and channel length must be uniform over fin height
- Conformal coverage required
- ALD technology has become critical for HK and MG layers
- **Pulsar® XP**
  - ALD for high-k
  - Cross-flow reactor
  - Solid source delivery system

- **EmerALD® XP**
  - ALD for metal gates
  - Showerhead reactor
What is Plasma Enhanced Atomic Layer Deposition (PEALD)?

Step 1: (Metal) Precursor Chemisorption

Step 2: Purge

Step 3: Reaction to Oxide/Nitride or metal with O,N,H Radicals

+ Faster
+ Lower temperatures
+ More chemistries
+ Denser films
- More complex
- Plasma may preclude some applications

and repeat…
Low temperature deposition of SiO₂ and Si₃N₄ opens up wide potential application space
New Materials enabling Lithography
Spacer Defined Double Patterning

Litho-formed Resist Pattern

44nm
Pitch

Conformal SiO$_2$

Anisotropic Etch

22nm
Pitch/2

Depo of SiO$_2$ at 50C

Left

Center

Right

Uniform CD's:
Spacer Thickness NU <1%, 3σ

ASM, ALD conference 2008; SPIE conference 2009
• **XP8**
  - High productivity single wafer tool for both PEALD and PECVD applications
  - Accommodates up to 8 chambers for PEALD or PECVD
  - PEALD and PECVD can be integrated on the same platform
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### Strong IP protected portfolio
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| Diffusion Furnace| • Smallest footprint per reactor  
• Low Cost of Ownership                                                                                                                                 |
| Epitaxy          | • Thick Epi layers for power devices  
• Strained Epi films for CMOS                                                                                                                                 |
| PECVD            | • Advanced intermetal dielectric film                                                                                                                                 |

### Strong IP protected portfolio

- ALD solution (Hafnium oxide)
- PEALD Low temp dielectrics
- Unique “dual reactor dual boat” design
- Epitaxial films for analog devices as well as for nMOS and pMOS
- Extreme low-k films
- Advanced intermetal dielectric film
- Thick Epi layers for power devices
- Strained Epi films for CMOS
- Advanced intermetal dielectric film

© 2013 ASM
• **Enabling transistor performance**
  • Strained epitaxial films for planar & FinFET devices

• **Excellent interface control for high quality film growth**
  • Integrated Pre-Clean module

• **High productivity**
  • Platform with 4 Epi chambers
  • Differentiated & patented high film growth processes
Epi layers for Power Devices
Multi-Layer Epi Technology

- Thick multi-layer epi needed for power management devices
- Number of epi layers depends upon the breakdown voltage required (Typical from 600 – 800V)
- Implemented in production by various companies

ASM Product: Epsilon® 3200
Epi for advanced power devices
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## PECVD

| • Extreme low-k films | • Advanced intermetal dielectric film |
| | |

## ASM Relative Positioning

- ✓ Leading IC manufacturers are customers
- ✓ ASM one of only two top vendors in PE-CVD low-k
- ✓ ASM one of only two top vendors

**Strong IP protected portfolio**
Extendibility of ASM’s Low-k Solution

- **Aurora® low-k (k=2.8~3.1)**
- **Aurora® low-k (k=2.6)**
- **Aurora® ELK (2.3-2.5)**
- **Aurora® ELK (2.0)**
- **UV-assisted process**

ILD k-value vs. Technology Node:
- 90~45nm
- 32nm
- 22nm
- 15nm
- 11nm
- 8nm
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**Strong IP protected portfolio**
**Productivity**
- One A412 PLUS = up to 80 kwpm (2.5 hr process, 95% available, 150 wafer boat)
- About 40% lower capex per m$^2$ as competitors
- Dual boat/dual reactor system

**Innovation**
- New ALD and CVD processes
- Example 1: AlN
- Example 2: very thin closed silicon, 3.5nm

Real time production data:

- WiW NU: $\sim$0.25% 1$\sigma$
Wafer Fab Equipment Forecast

Share of 28nm, 22nm and 14nm of total Equipment spending increasing in 2013-2014

Key customer ALD penetrations in 28, 22 and 14nm: market segments with high expected growth

Gartner June, 2013
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Summary and Conclusions

- Scaling is increasingly enabled by new materials and 3D technologies
- ALD enables new materials and 3D
- The ALD market offers strong growth opportunities
- Adoption of more ALD and PEALD applications in HVM continues
  - ASMI #1 position in ALD for High-k gate
  - 3D FinFET’s drive adoption of ALD, not only for the dielectric, but also for metals
  - Strengthening inroads with PEALD on XP8, high productivity system for PEALD and PECVD applications
- Intrepid® XP, system with 4 Epi reactors, targeting strained Epi layers for CMOS
- ASM’s Vertical Furnace is providing low CoO and footprint per reactor
Drive Innovation, Deliver Excellence