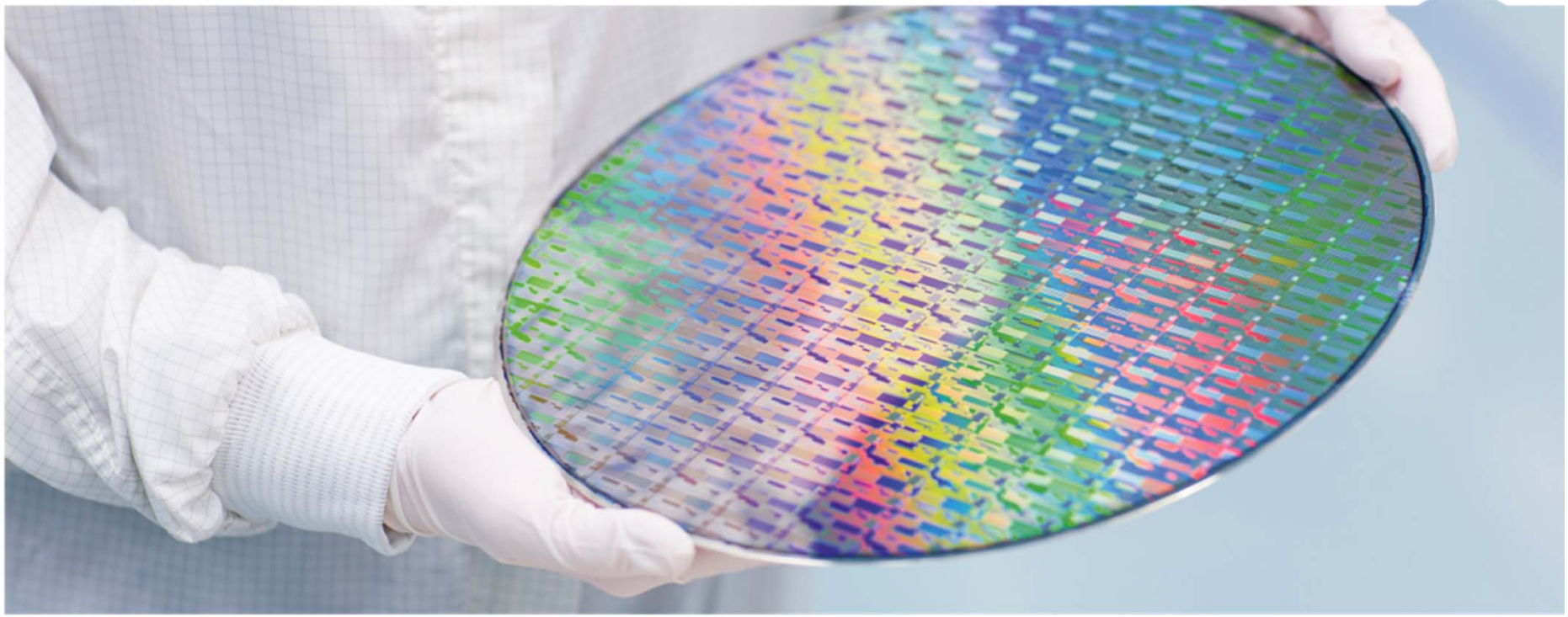
DRIVE INNOVATION · DELIVER EXCELLENCE >

ASM



ADVANCED WAFER PROCESSING WITH NEW MATERIALS

ASM International
Analyst and Investor Technology Seminar
Semicon West July 15, 2015

SAFE HARBOR STATEMENTS

Safe Harbor Statement under the U.S. Private Securities Litigation Reform Act of 1995: All matters discussed in this business and strategy update, except for any historical data, are forward-looking statements. Forward-looking statements involve risks and uncertainties that could cause actual results to differ materially from those in the forward-looking statements. These include, but are not limited to, economic conditions and trends in the semiconductor industry generally and the timing of the industry cycles specifically, currency fluctuations, corporate transactions, financing and liquidity matters, the success of restructurings, the timing of significant orders, market acceptance of new products, competitive factors, litigation involving intellectual property, shareholder and other issues, commercial and economic disruption due to natural disasters, terrorist activity, armed conflict or political instability, epidemics and other risks indicated in the Company's filings from time to time with the U.S. Securities and Exchange Commission, including, but not limited to, the Company's reports on Form 20-F and Form 6-K. The company assumes no obligation to update or revise any forward-looking statements to reflect future developments or circumstances.

OUTLINE

- **New Materials and 3D: Moore's law enablers**
- **ASM and New Materials**
  - ALD as enabler of new materials
  - ASM New Materials development strategy
  - ALD supply chain components
- **ASM Products and selected applications**
- **Summary and Conclusions**

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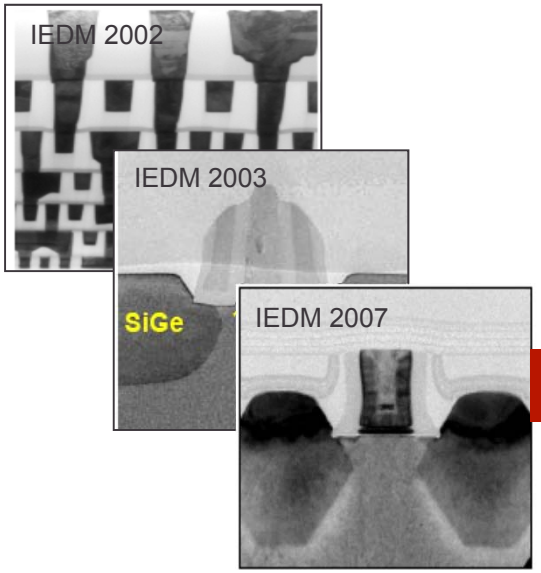
SCALING IS INCREASINGLY ENABLED BY NEW MATERIALS AND 3D TECHNOLOGIES

1990 1995 2000 2005 2010 2015 2020 2025

Scaling enabled by Litho

Patterning Spacers



Scaling enabled by Materials

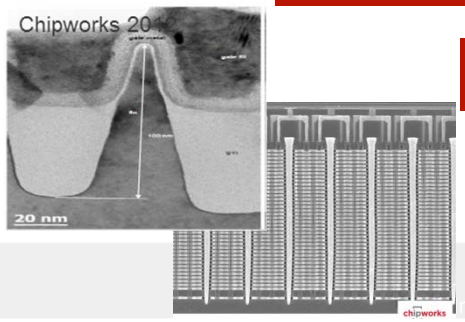
Low-k

Strained Si

High-k

High-mobility Materials

Scaling enabled by 3D



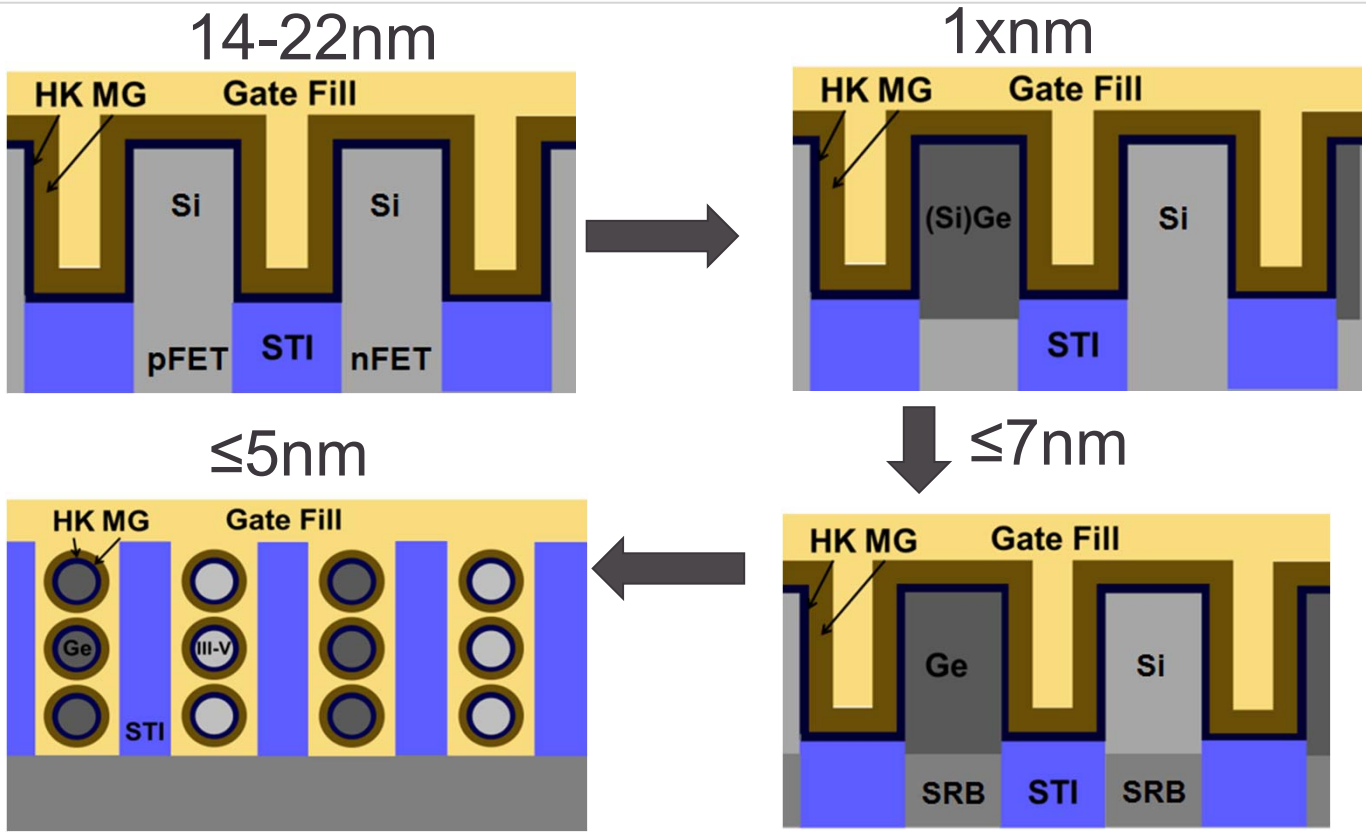
FinFET

3D TSV

3D Memory

GAA

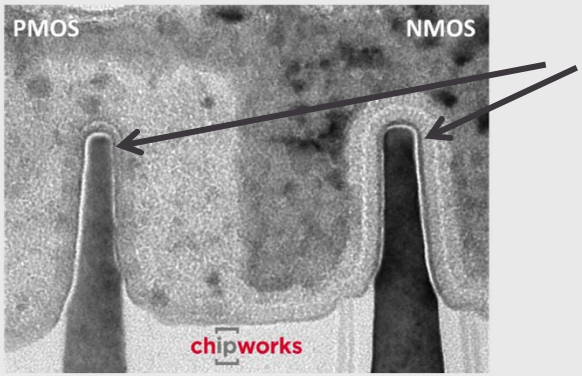
SCALING BY MATERIALS AND 3D



- **Density scaling (continuing Moore's law) driving towards higher mobility materials and alternate device architectures**
- **Future systems will integrate much wider variety of materials and device structures**

NEW MATERIALS AND PROCESSES: MOORE'S LAW ENABLERS

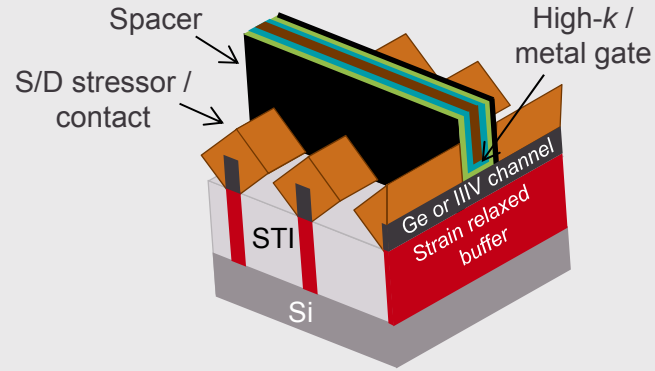
Higher Capacitance, Lower Leakage



High-k / Metal Gate

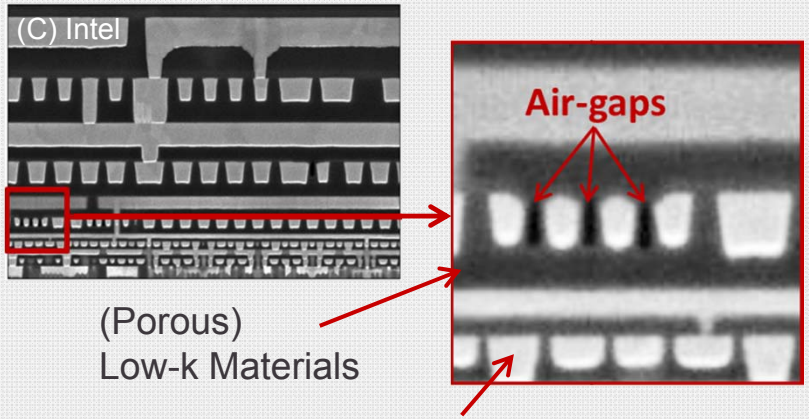
DRAM, RF, decoupling capacitors

Higher Mobility, Lower Resistance

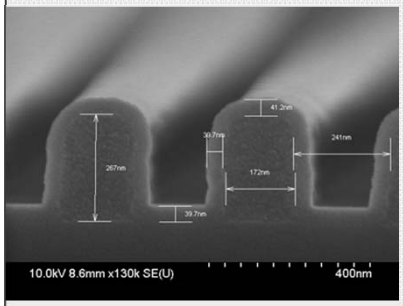


Strain and new Channel Materials
New metal contacts

Less Cross Talk, Faster Interconnect



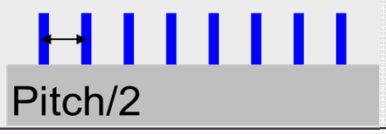
Smaller Feature Sizes



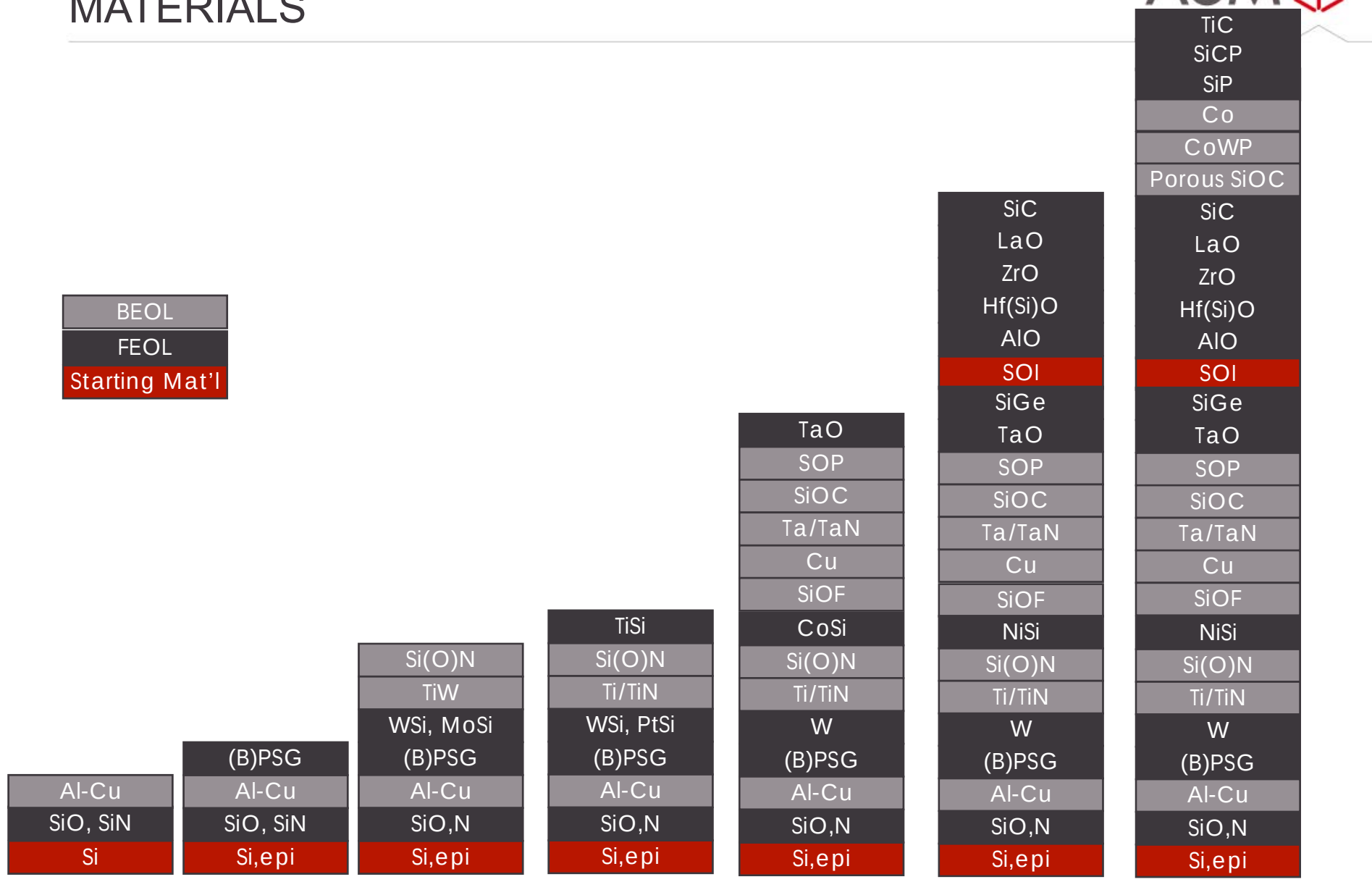
Sub-Rayleigh limit patterning using SDDP

Conformal SiO_2

Anisotropic Etch



INCREASING INTRODUCTION RATE OF NEW MATERIALS



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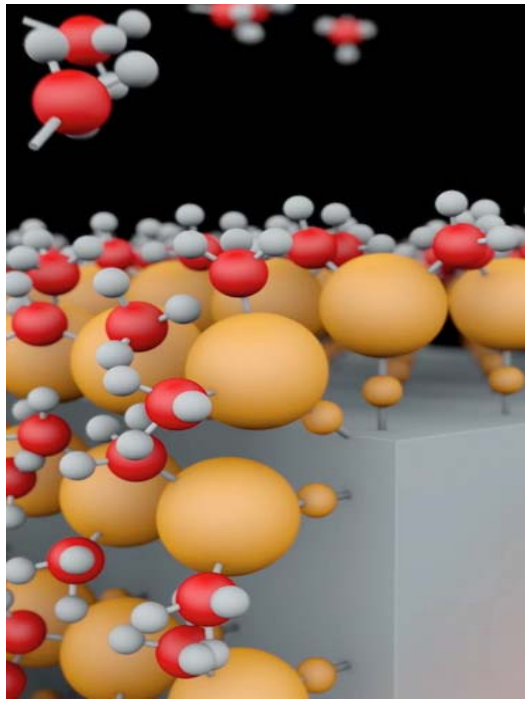
ASM AND NEW MATERIALS

- **ASM technology focuses on enabling new materials and new device integration roadmaps**
  - 3D transistor formation (FinFET & beyond FinFET)
  - DRAM, Flash and emerging memory
  - More than Moore / IoT applications (MEMS, Sensors, Power)
- **ALD and PEALD as enablers of new materials**
  - ALD high-k metal gates
  - PEALD low temp spacers for multi-patterning
  - Other emerging applications



ALD AS ENABLER OF NEW MATERIALS - KEY STRENGTHS OF ALD

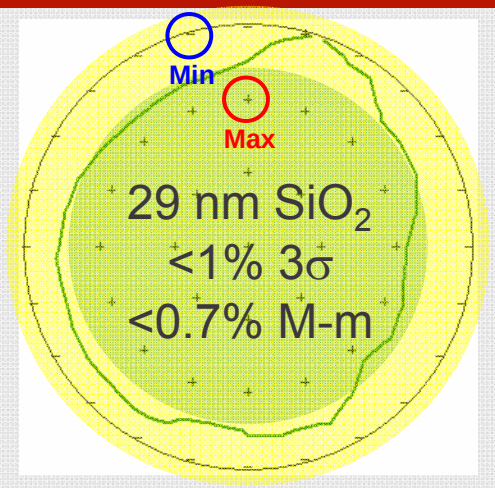
Uniformity

Wafer Statistics

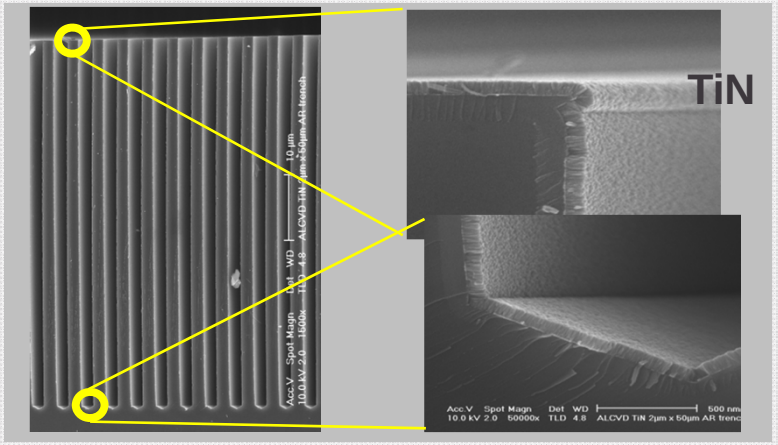
Mean:	291.0183
Maximum:	292.6831
Minimum:	288.7532
Std. Dev:	0.9647908
	0.33 %
Range:	3.9299
Hi/Lo Var:	0.68 %
Unit:	

Wafer Size

Wafer Diam:	300.00 mm
Test Diam:	296.00 mm
No. Sites:	49
Style:	Notch

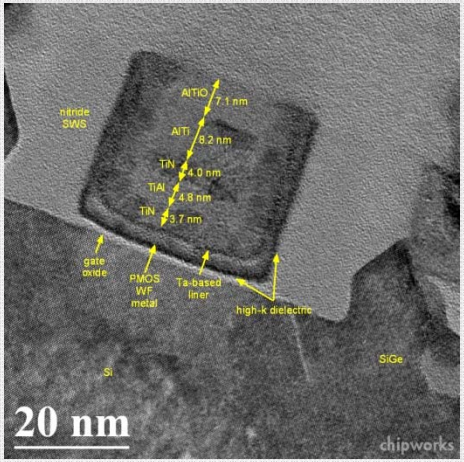


Step Coverage



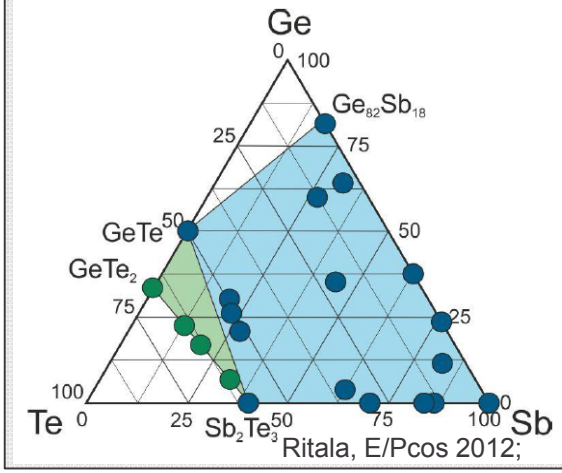
SEM's Courtesy of Philips Research Labs

Interface Control



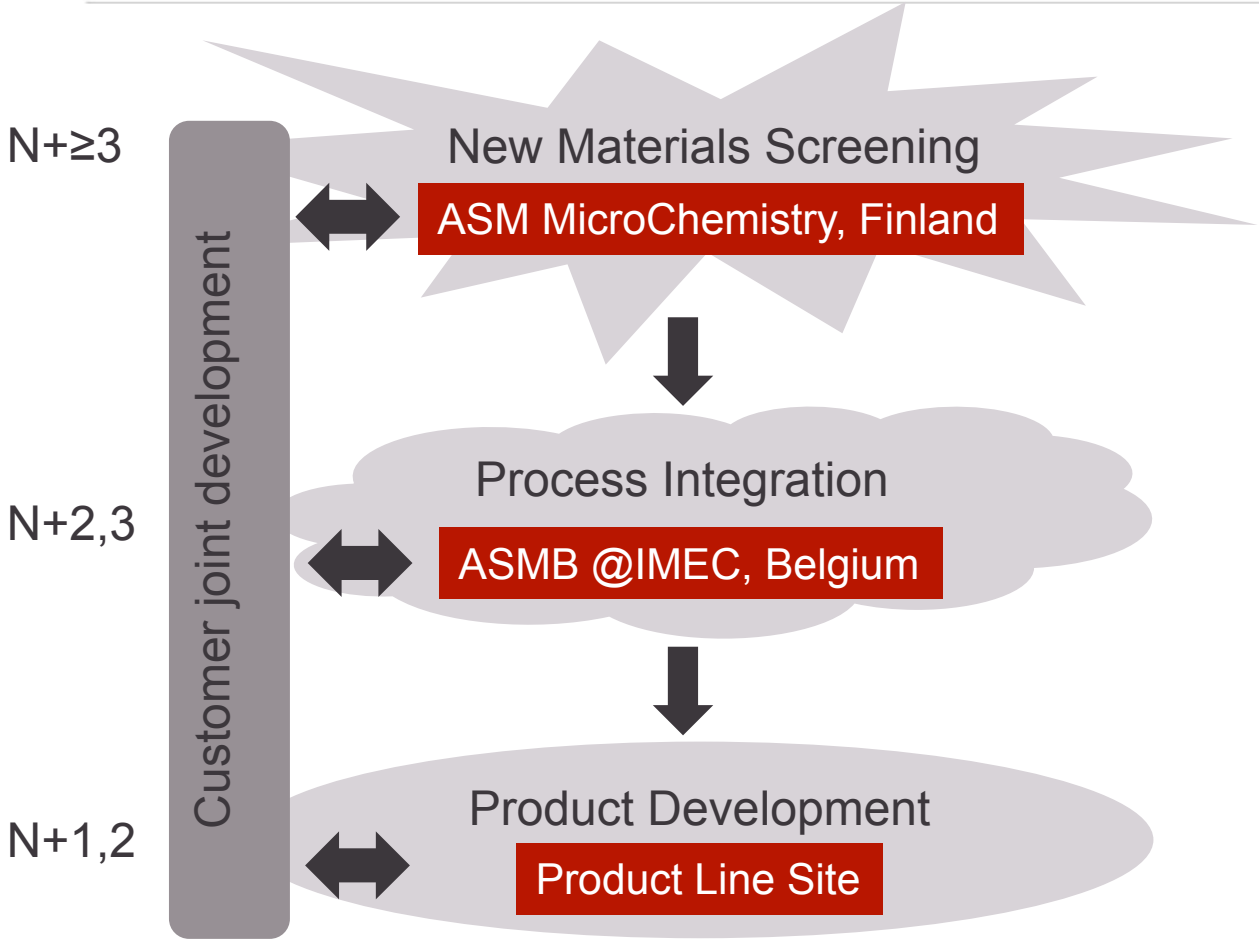
Atomically engineered interfaces to optimize leakage current, reliability and work-functions

Composition Control



Excellent composition control for ternary alloys; all ALD solution demonstrated for GST

ASM NEW MATERIALS DEVELOPMENT STRATEGY



- Basic materials R&D
- Chemical synthesis
- Pre-cursor screening

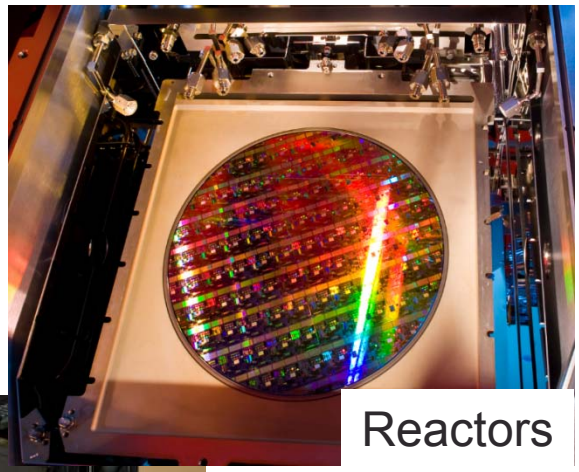
- Process development
- Integration
- Device characterization

- Engineering
- Product development
- Product marketing

CRITICAL ALD SUPPLY CHAIN COMPONENTS

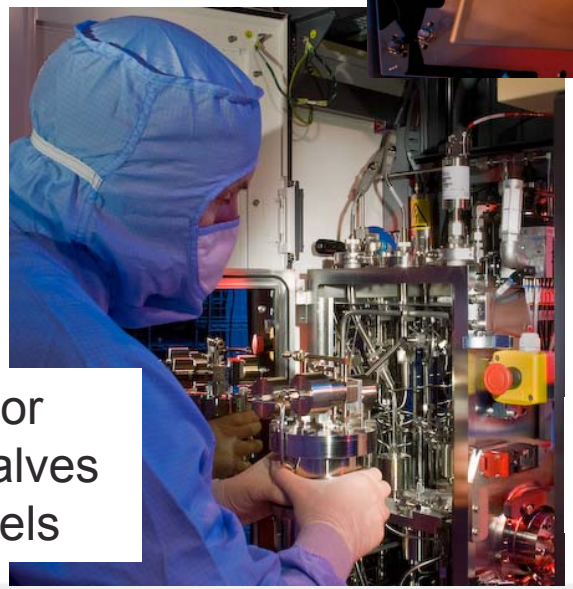
Fundamental Capability → Process Performance → Productivity → Integrated Process → Final Product Capability

Pre-cursors



Reactors

High productivity tools



Pre-cursor Delivery, Valves and Vessels

Fab facilities, pumps & abatement

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ASM PRODUCTS
ALD

› Pulsar® XP

- ALD for high-k
- Cross-flow reactor
- Solid source delivery system

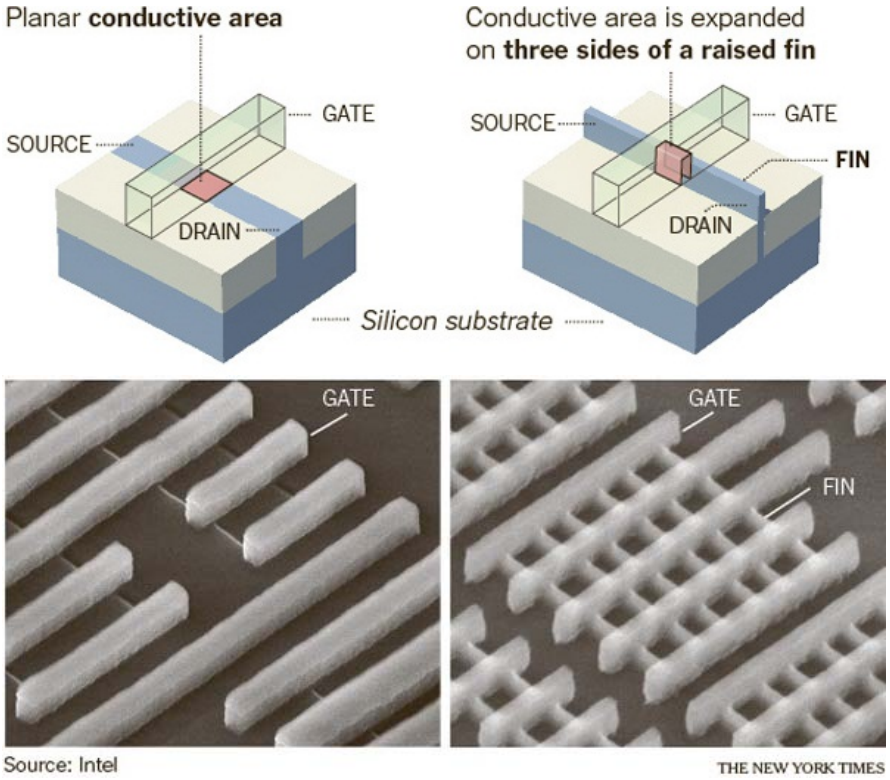
Pulsar® XP

› EmerALD® XP

- ALD for metal gates
- Showerhead reactor

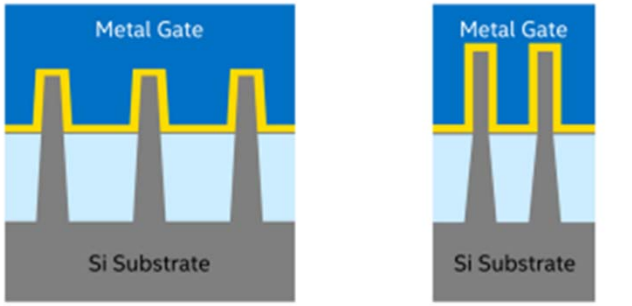
EmerALD® XP

FINFET CHALLENGES:
ALD ENABLES FURTHER SCALING IN 3D



Source: Intel

THE NEW YORK TIMES



22 nm 1st Generation Tri-gate Transistor

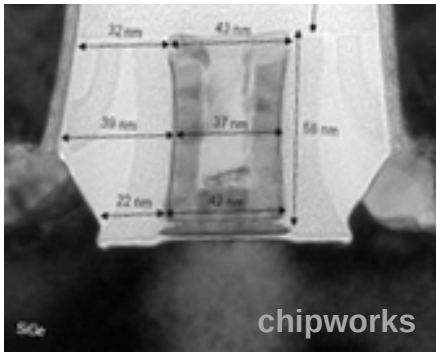
14 nm 2nd Generation Tri-gate Transistor

	22 nm Node	14 nm Node	Scale
Transistor Fin Pitch	60	42	.70x
Transistor Gate Pitch	90	70	.78x
Interconnect Pitch	80 nm	52 nm	.65x

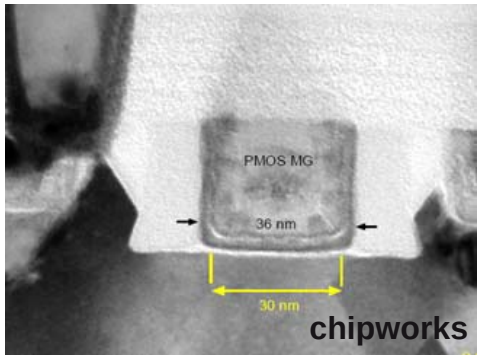
Source: Intel

- Materials properties and channel length must be uniform over fin height
- Conformal coverage required
- Aspect ratios increase going from 22nm to 14nm
- → ALD technology has become critical for HK and MG layers

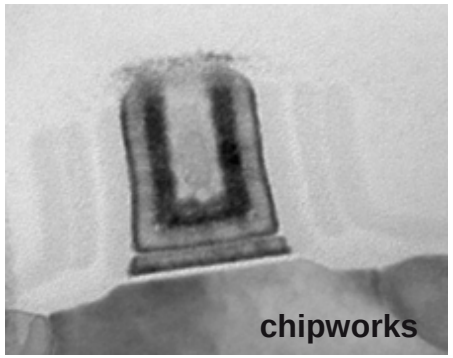
EXTENDIBILITY OF HAFNIUM BASED OXIDES



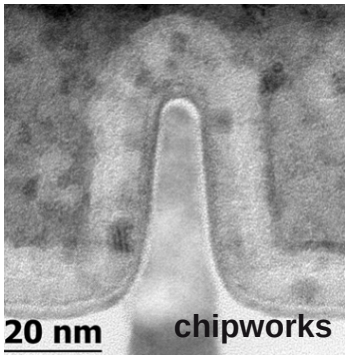
45nm HK first RPMG
Planar FET



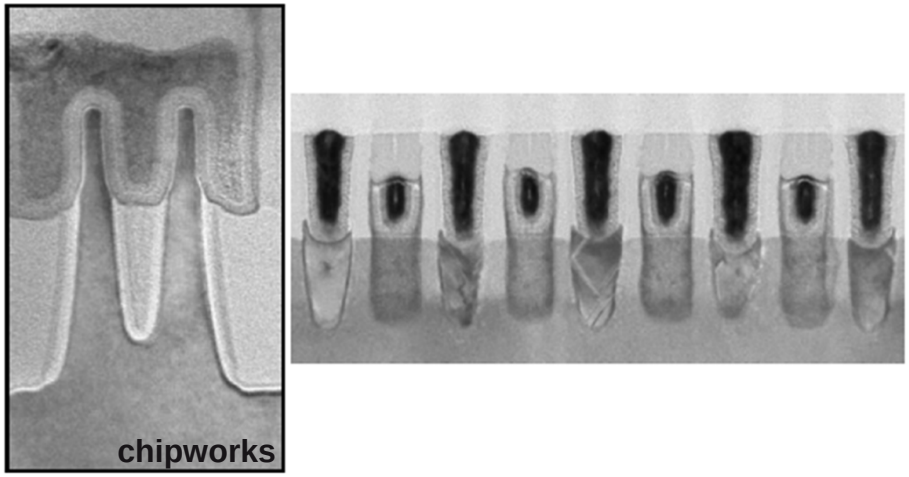
32 nm HK last RPMG
Planar FET



28nm HK first RPMG
Planar FET



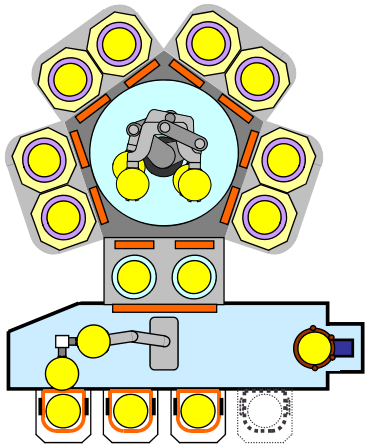
22nm HK last RPMG
FinFET



14nm HK last RPMG
FinFET

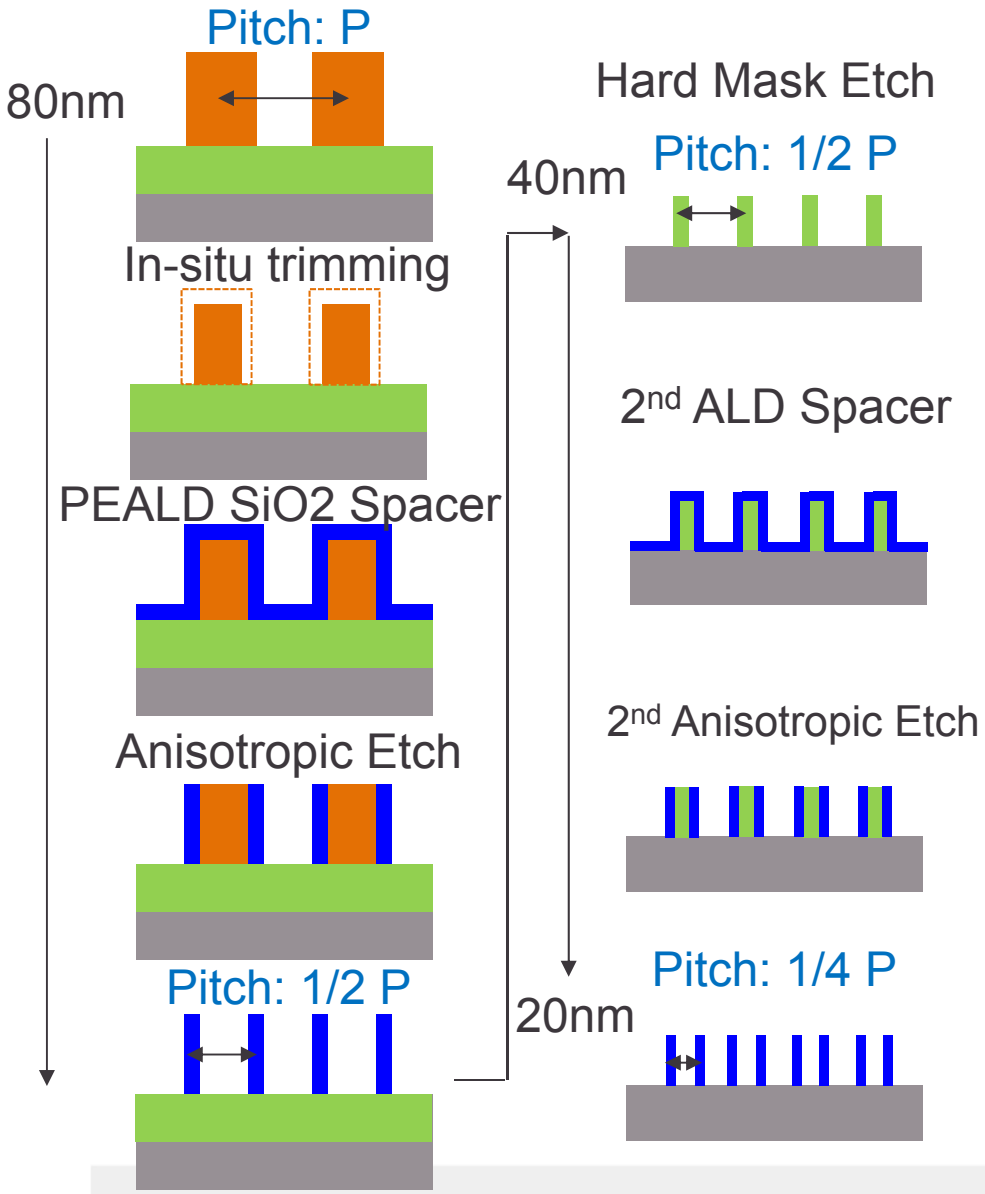
XP8-DCM

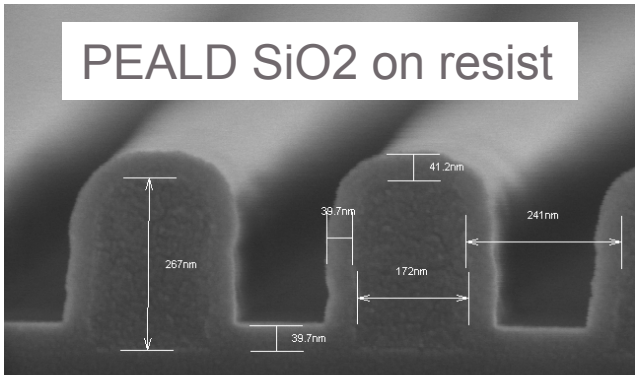
- High productivity single wafer tool for both PEALD and PECVD applications
- Accommodates up to 8 chambers by DCM
- PEALD and PECVD can be integrated on the same platform



DCM (Dual Chamber Module)

ALD ENABLING SUB-RAYLEIGH LIMIT LITHOGRAPHY WITH SPACER DEFINED DOUBLE/QUADRUPLE PATTERNING





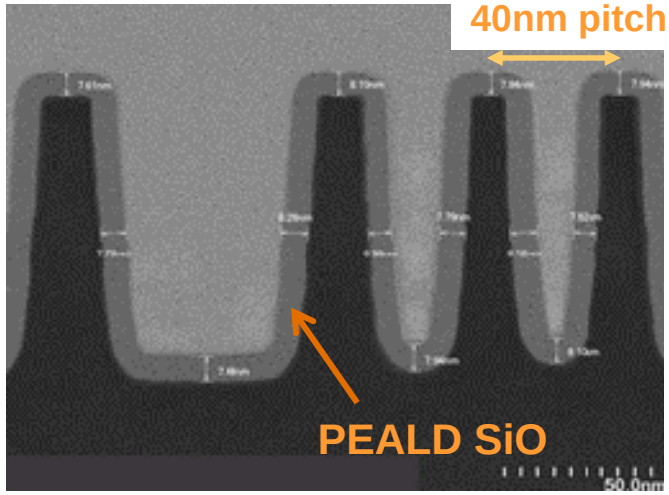
- ✓ **Spacer Defined Double Patterning with PEALD in production since 3x nm DRAM and Flash**
- ✓ **Spacer Defined Quadruple Pattering in production for 1x nm Flash**

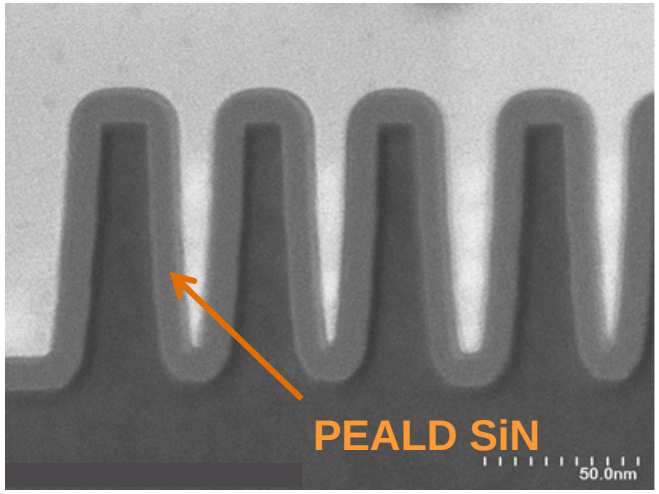
Key enablers brought by PEALD

- Uniformity: CD control
- Low temperatures (<100C)
- Good step coverage
- Dense film
- In-situ trimming capability
- Extendible to other materials with high etch selective

PEALD SiO_2 and Si_3N_4 permanent spacers

- Low temperature (300 ~ 550 °C)
- High conformality
- High quality (low WER, low leakage current)

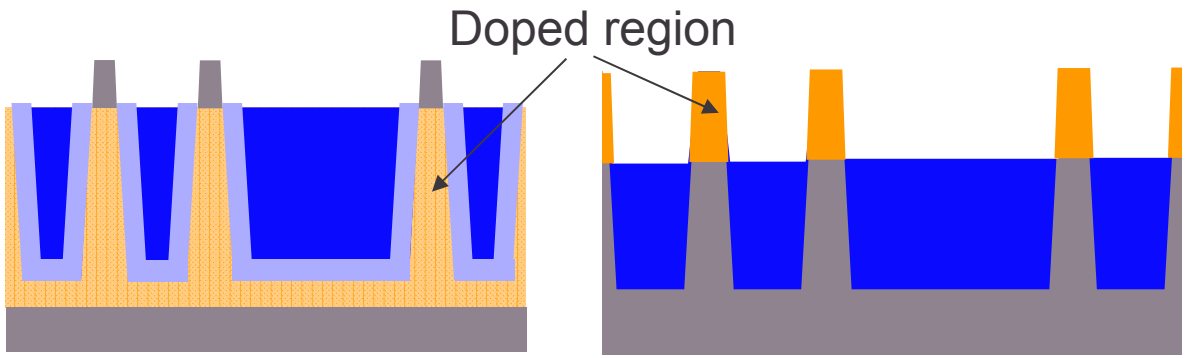




PEALD DOPED OXIDES; SOLUTION FOR FINFET DOPING

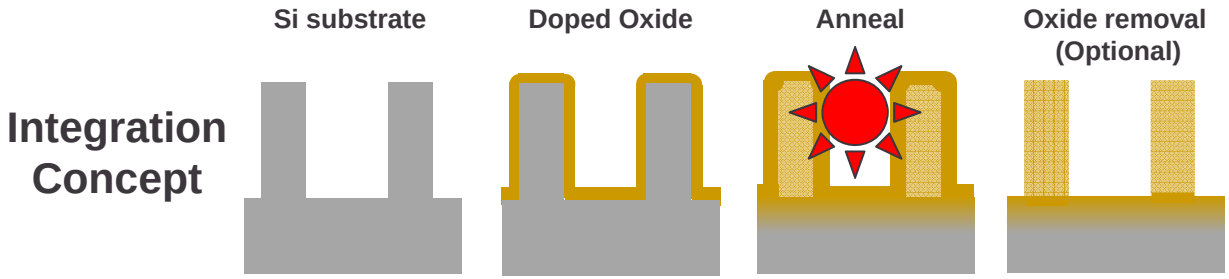
BENEFITS:

- Ability to dope selective regions in **vertical** direction
- Low damage / substrate consumption vs. Ion Implant



Process Flow 1
"**Bottom** Fin Doping"
Subfin doping for
punch-through stopper

Process Flow 2
"**Top** Fin Doping"
Channel/SD extension



ASM PRODUCTS
ADVANCED EPITAXY

Advanced transistors enabled with Intrepid® XP

- Relaxed & strained epitaxy for Si, SiGe & Ge based FinFETs through 7nm
- Channel (SRBs), S/D stressor, contact & passivation cap layer

Integrated, low thermal budget pre-clean module

- High quality surface with low interface contamination

High productivity & lowest CoO

- XP Platform with up to 4 process modules
  - Flexible configuration with pre-clean (3+1& 2+2)
- Differentiated film growth processes enabling devices with high drive currents & best-in-class productivity
- High throughput with pulsed Epi processes & high doping levels

Intrepid® XP

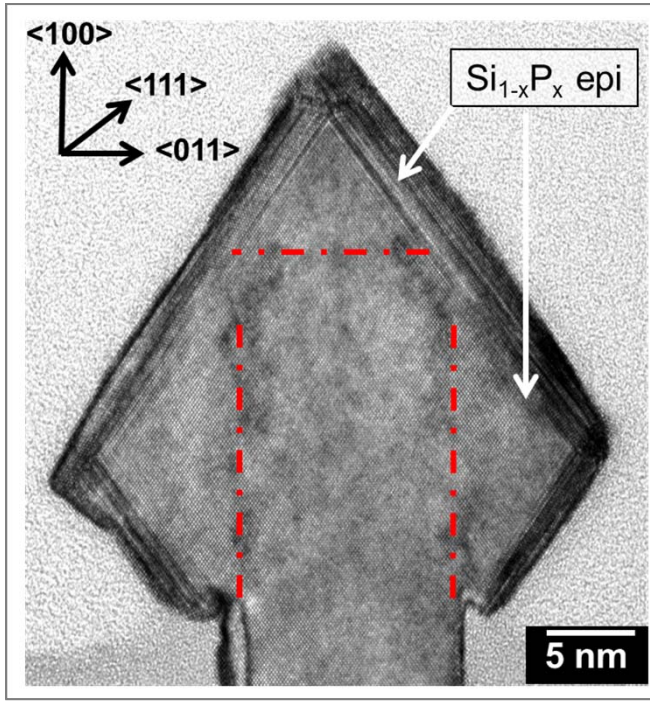
EPI SI:P PROCESS FOR FINFET

Epitaxial SiP film for nMOS FinFETs

Key Challenges

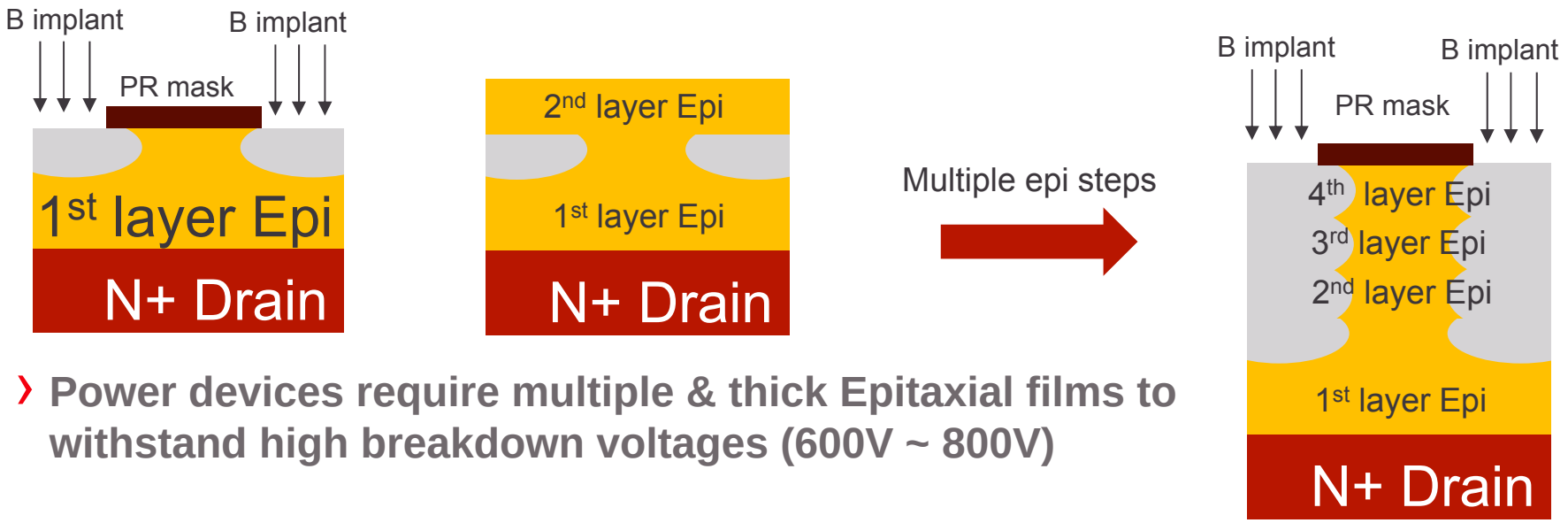
- Selective Epi process
- High P doping levels (>1E21) for lower resistivity. P concentration requirement increases at each node.
- Thickness and dopant uniformity and repeatability
- Low defects
- Throughput, especially at lower temps

Integrated preclean required for pre-epi surface control



J. Tolle, *et. al*., ECS 2012.

EPI LAYERS FOR POWER DEVICES
MULTI-LAYER EPI TECHNOLOGY



- **Power devices require multiple & thick Epitaxial films to withstand high breakdown voltages (600V ~ 800V)**
- **Breakdown voltage of the device dictates number of Epi layers needed**
- **Doping level and uniformity of the Epi layers is critical and an ASM advantage**
- **In HVM at several power device manufacturers enabled by:**

ASM Product: Epsilon® 3200

ASM PRODUCTS
FURNACE CVD /DIFFUSION /BATCH ALD

A412 PLUS

- Dual boat/dual reactor system
- Clustering of different applications between reactors possible – only vertical furnace in the market with this capability
- Up to 150 product wafer load size
- New stocker design with integrated N2-FOUP purge and 36 FOUP positions

Applications:

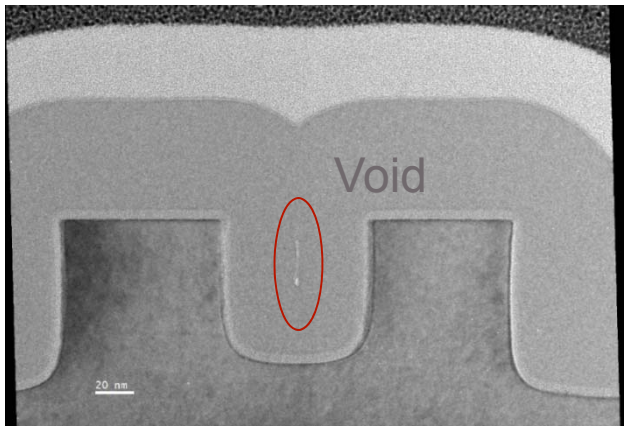
- Full range of applications for Logic, Memory, Power and MEMS

- LPCVD Silicon, SiN, TEOS, HTO
- Diffusion, Anneal, Cure, Reactive Cure
- Pulsed CVD and Batch ALD (AlO, AlN, TiN, SiN, SiO etc)

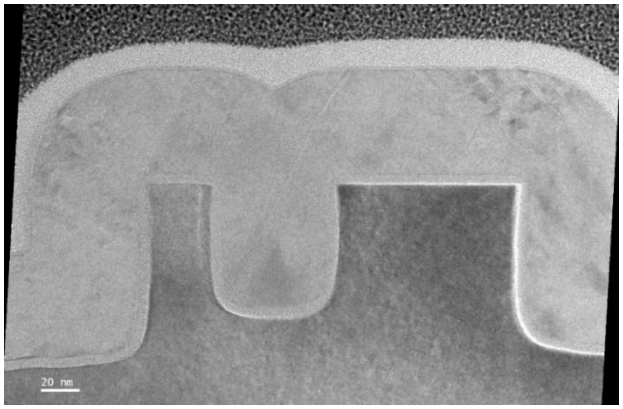
A400/A412 FURNACE - INNOVATION

Example 1: Voidless silicon gapfill.

- Filling of trenches of rectangular shape imposes challenge for voidless gapfill in >14nm.
- Standard silicon gap fill:

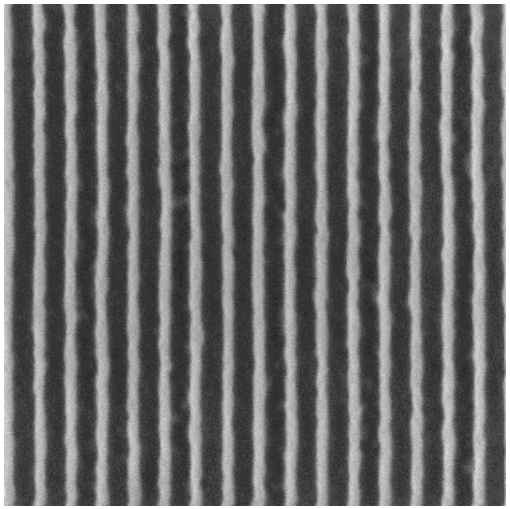


- ASM solution. Voidless silicon gap fill:

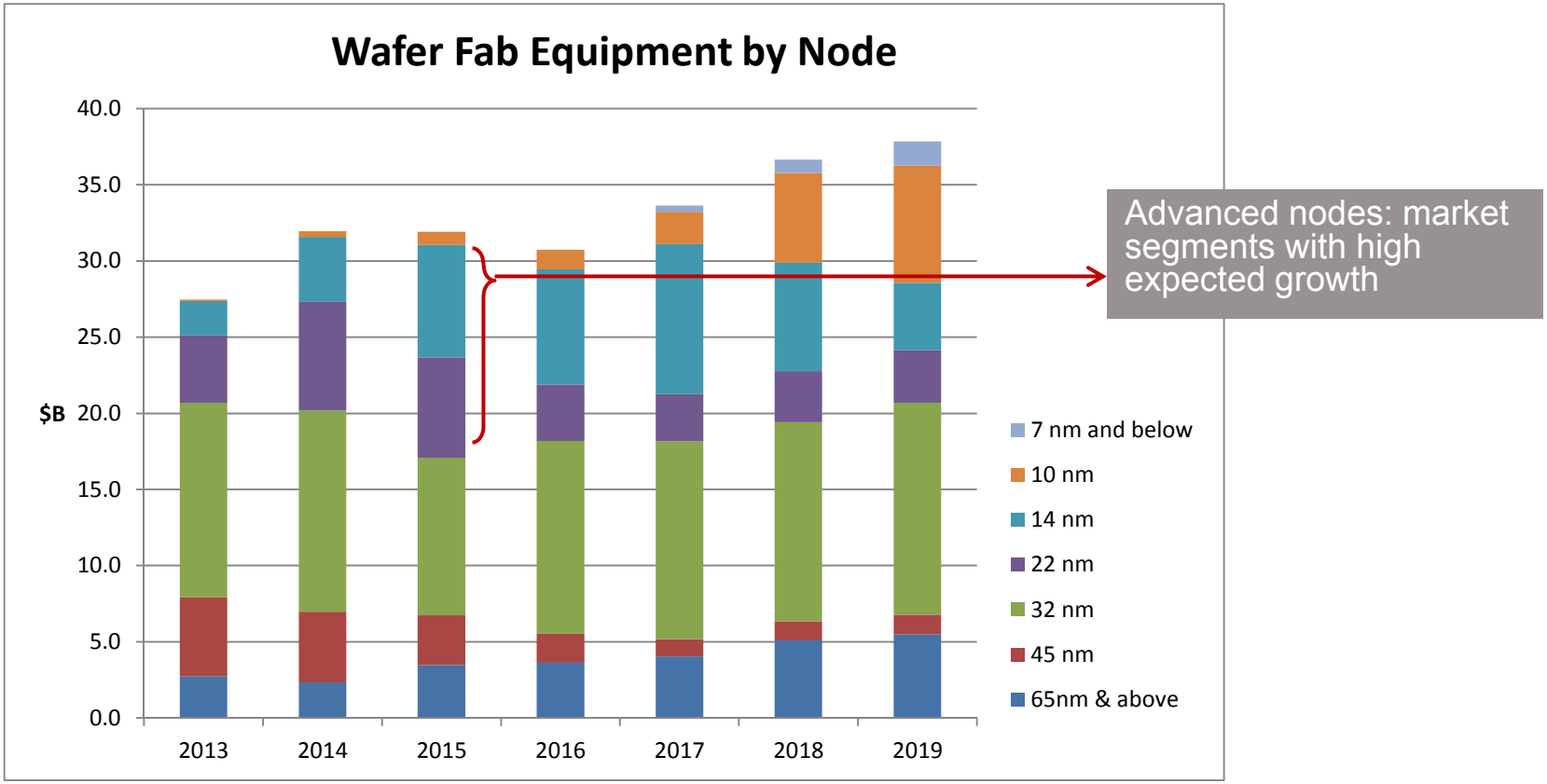


Example 2: ALD assisted Directed Self Assembly (DSA)

- DSA is a promising patterning technique for 7nm and beyond
- Combining DSA with Selective ALD boosts the etch resistance of DSA polymers and reduces Line Etch Roughness by >40%
- Parallel lines of selective Al2O3 deposited on A412 furnace, 14 nm half pitch (SPIE conference, 2015):



WAFER FAB EQUIPMENT FORECAST



Gartner July, 2015

Key customer ALD and PEALD penetrations in 14nm and 10nm: market segments with high expected growth

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SUMMARY AND CONCLUSIONS

- Scaling is increasingly enabled by new materials and 3D technologies
- ALD and PEALD enable new materials and 3D
- Hafnium based ALD high-k gates on ASM Pulsar® extendable for 4 device generations
- XP8 PEALD patterning films continue to be extendable
- XP8 PEALD Doped oxides solution for fin doping
- Intrepid® XP, system with up to 4 Epi reactors, targeting strained Epi layers for CMOS, and Epsilon® 3200 for analog/power
- ASM's Vertical Furnace is providing high productivity, in combination with continued process innovation

DRIVE INNOVATION • DELIVER EXCELLENCE