DRIVE INNOVATION · DELIVER EXCELLENCE >

HIGH PRODUCTIVITY SOLUTIONS FOR ADVANCED WAFER PROCESSING WITH NEW MATERIALS

ASM International
Analyst and Investor Technology Seminar
Semicon West July 10, 2018

CAUTIONARY NOTE

Cautionary Note Regarding Forward-Looking Statements: All matters discussed in this presentation, except for any historical data, are forward-looking statements. Forward-looking statements involve risks and uncertainties that could cause actual results to differ materially from those in the forward-looking statements. These include, but are not limited to, economic conditions and trends in the semiconductor industry generally and the timing of the industry cycles specifically, currency fluctuations, corporate transactions, financing and liquidity matters, the success of restructurings, the timing of significant orders, market acceptance of new products, competitive factors, litigation involving intellectual property, shareholders or other issues, commercial and economic disruption due to natural disasters, terrorist activity, armed conflict or political instability, epidemics and other risks indicated in the Company's reports and financial statements. The Company assumes no obligation nor intends to update or revise any forward-looking statements to reflect future developments or circumstances.

OUTLINE

- **New Materials and 3D: Moore's law enablers**
  - ASM technology focus: enabling new materials and new device integration roadmaps
  - Logic scaling
  - Memory scaling
- **ALD**
  - ASM ALD Products
  - Selected applications in Logic, 3D-NAND, DRAM and Emerging Memory
- **PECVD**
- **Epitaxy**
- **Vertical Furnace**
- **ALD – Introducing Synergis®**
  - Synergis features & benefits

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MOORE'S LAW IS INCREASINGLY ENABLED BY NEW MATERIALS AND 3D TECHNOLOGIES

1990 1995 2000 2005 2010 2015 2020 2025

Scaling enabled by Litho

IEDM 2002

IEDM 2003

SiGe

IEDM 2007

Patterning Spacers

Multi-Color ESL Self-aligned

Scaling enabled by Materials

Low-k

Strained Si

High-k

High-mobility Materials

Scaling enabled by 3D

Chipworks 20

20 nm

FinFET

3D TSV

CFET

3D Memory

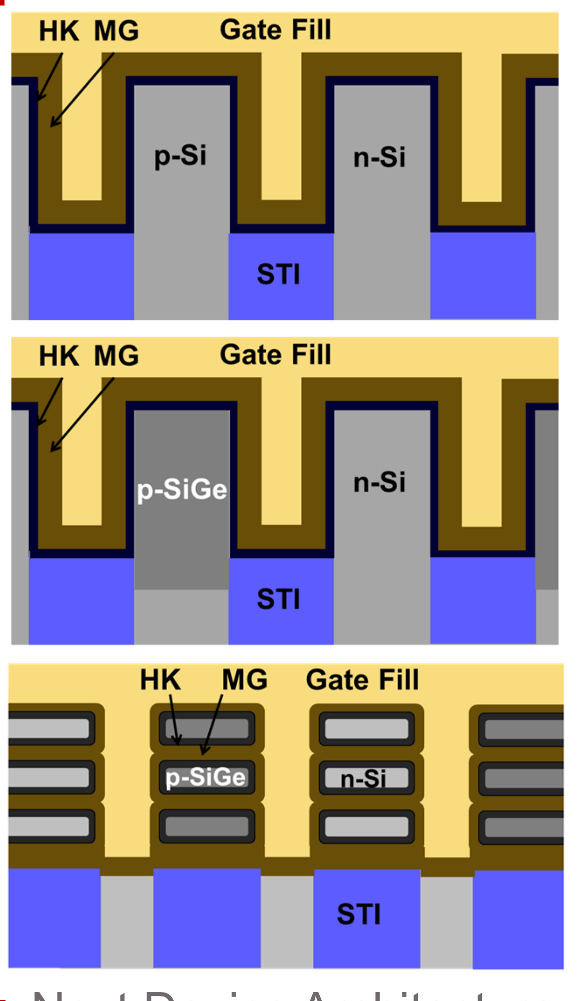
HGAA

3D CMOS

LOGIC SCALING BY MATERIALS AND 3D

2011

FinFET Device



~2023

Next Device Architecture – Horizontal Gate All Around

- **Density scaling (continuing Moore's law) driving towards higher mobility, lower resistivity and very conformal materials**
- **Future systems will integrate much wider variety of materials**
- **New device architectures will be needed around N3**

MEMORY SCALING BY MATERIALS AND 3D

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ASM PRODUCTS
ALD

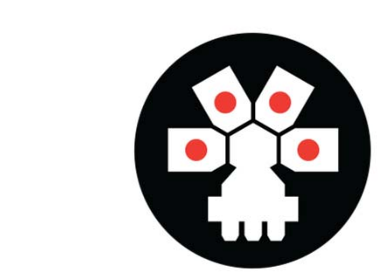
› Pulsar® XP

- ALD Hf based high-k gate dielectrics
- ALD metal oxides for etch stops, liners and pattern assist layers
- Cross-flow reactor
- Solid source delivery system

Pulsar® XP

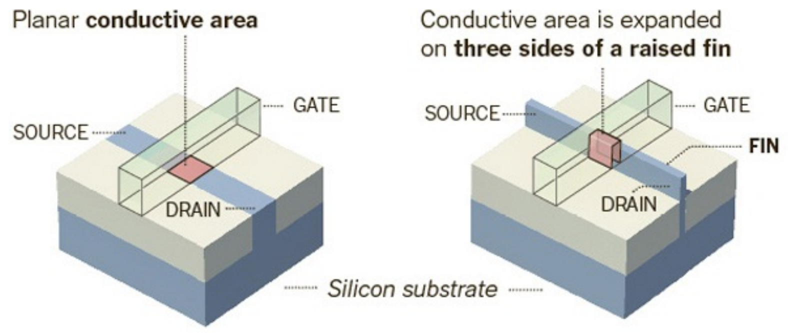
› EmerALD® XP

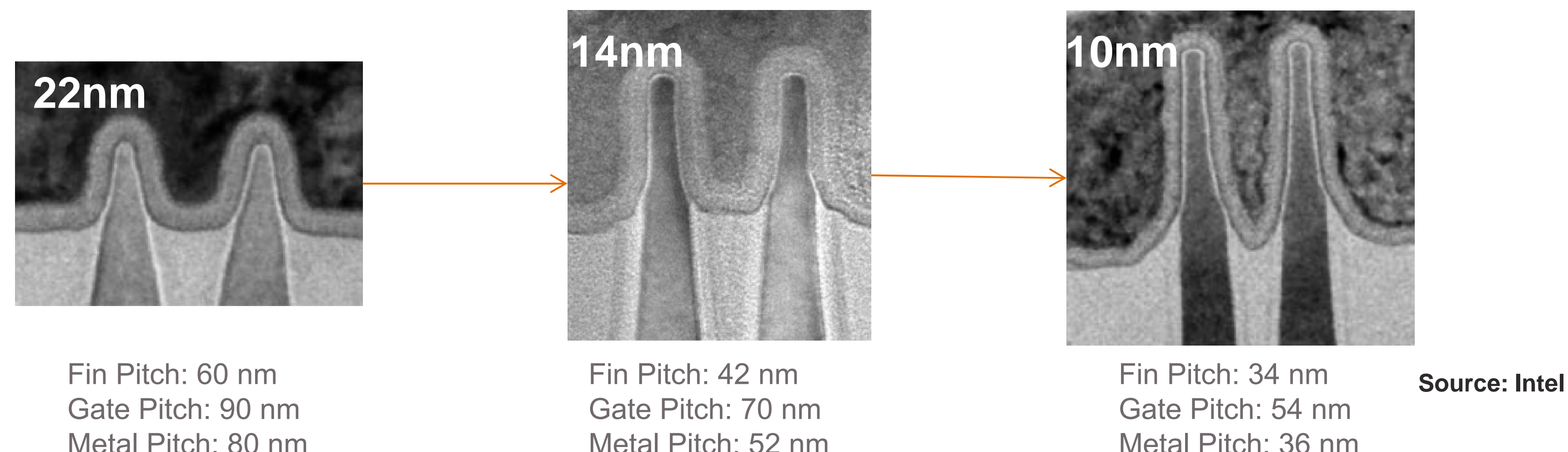
- ALD metal gate electrodes
- ALD metal nitrides for capacitor electrodes
- Showerhead reactor



EmerALD® XP

FINFET CHALLENGES:
ALD ENABLES FURTHER SCALING IN 3D





Fin Pitch: 60 nm
Gate Pitch: 90 nm
Metal Pitch: 80 nm

Fin Pitch: 42 nm
Gate Pitch: 70 nm
Metal Pitch: 52 nm

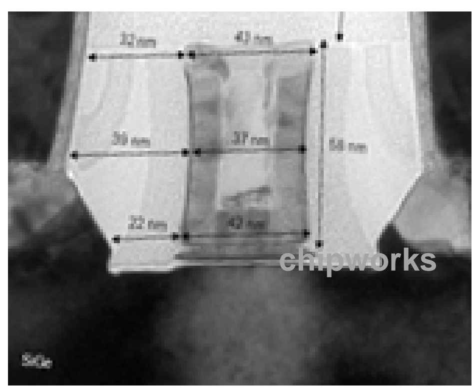
Fin Pitch: 34 nm
Gate Pitch: 54 nm
Metal Pitch: 36 nm

Source: Intel

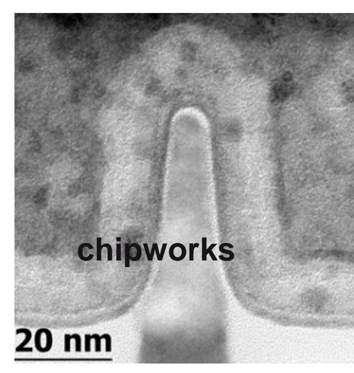
- Materials properties and channel length must be uniform over fin height
- Conformal coverage required
- Aspect ratios increase going from 22nm to 14nm to 10nm

  → ALD technology remains critical for HK and MG layers

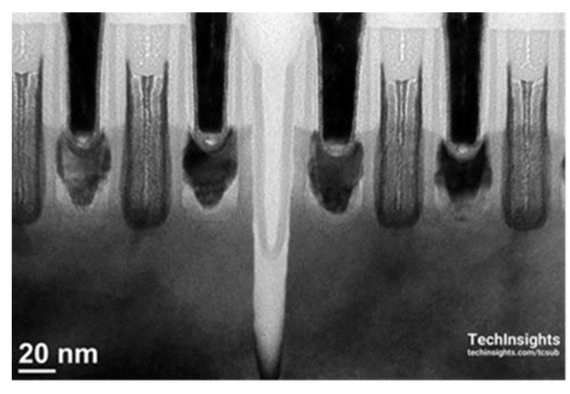
EXTENDIBILITY OF HAFNIUM BASED GATE OXIDE AND METAL GATE TECHNOLOGY



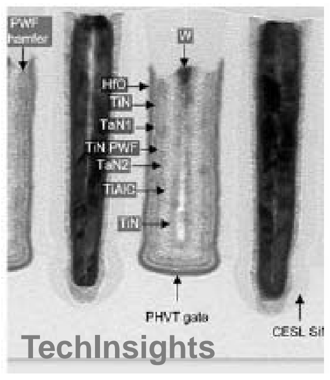
45nm HK first RPMG
Planar FET

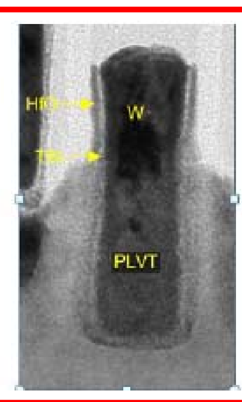


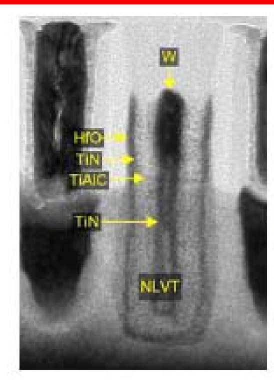
22nm HK last RPMG
FinFET

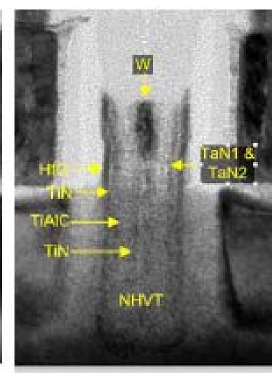


10nm HK last RPMG
FinFET plus additional HK tuning layer









10nm multi-work function metal gate stack

XP8-DCM

- High productivity single wafer tool for both PEALD and PECVD applications
- Accommodates up to 8 chambers by DCM
- PEALD and PECVD can be integrated on the same platform

DCM (Dual Chamber Module)

PEALD FOR SPACER DEFINED DOUBLE/QUADRUPLE PATTERNING

Pitch: P

In-situ trimming

PEALD SiO2 Spacer

Anisotropic Etch

Pitch: 1/2 P

Hard Mask Etch

Pitch: 1/2 P

2nd ALD Spacer

Pitch: 1/4 P

ALD SiO2 on resist

ALD MOx on resist

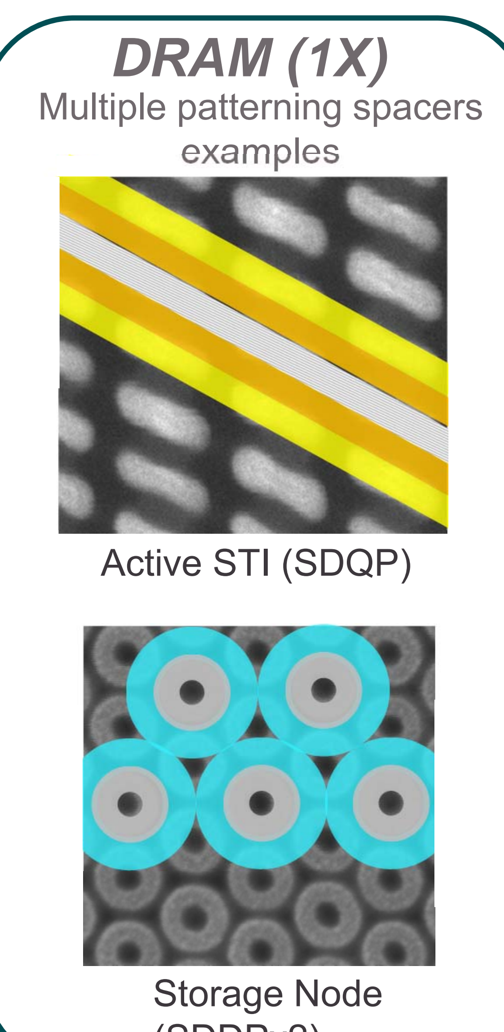
- ✓ Spacer Defined Double Patterning (SDDP) with ALD in production since 3xnm DRAM, in 3D-NAND and Emerging Memory
- ✓ Spacer Defined Quadruple Pattering (SDQP) in production for 1xnm DRAM
- ✓ SDDP/SDQP qualified with 10nm/7nm Logic customers

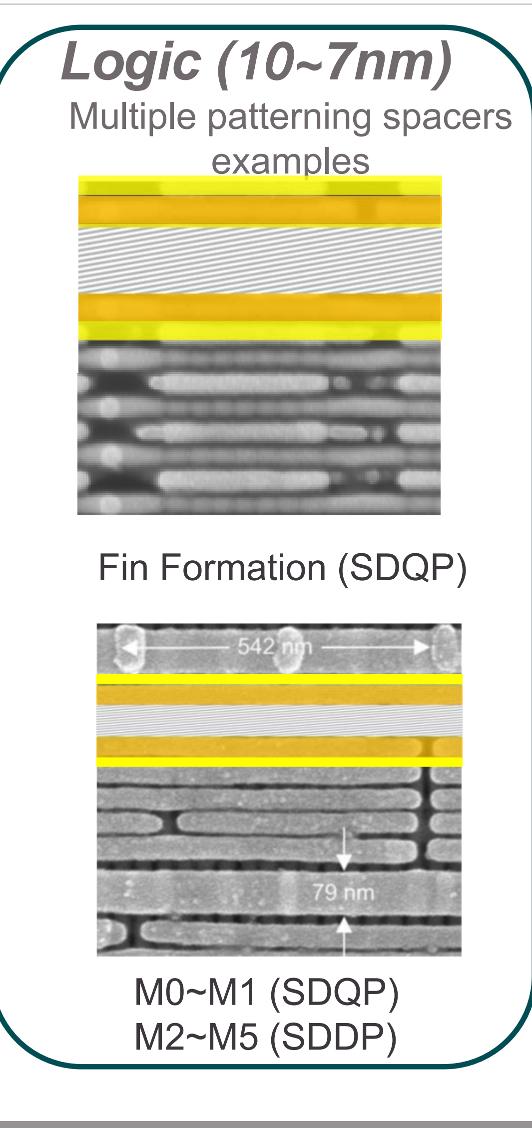
Key enablers brought by ALD

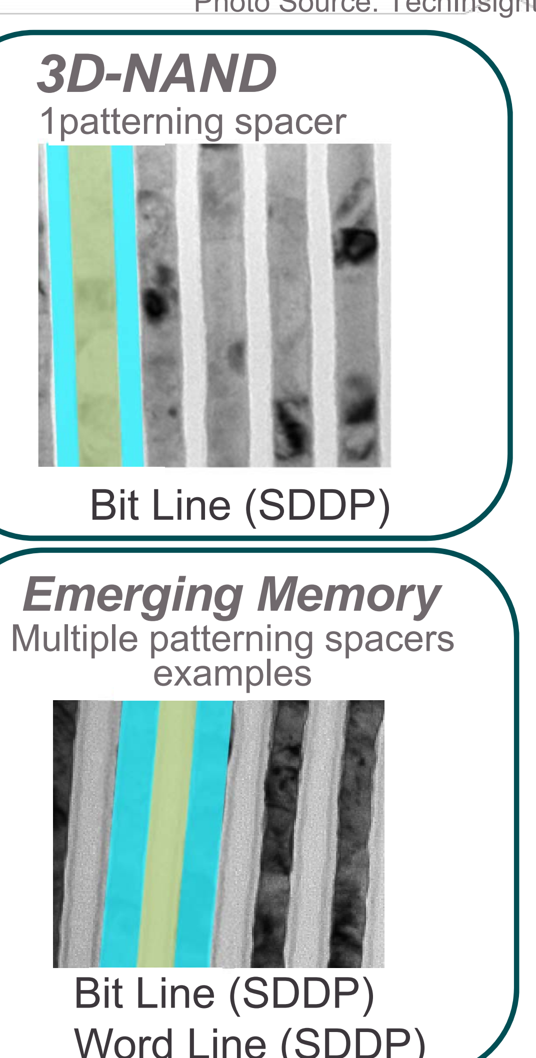
- Uniformity: CD control
- Low temperatures (<100C)
- Good step coverage
- In-situ trimming capability
- Extendible to other materials with etch selectivity
  → MOx shows different etch contrast and better mechanical properties compared to SiO, valuable for SDXP

CURRENT ALD PATTERNING SPACER APPLICATIONS

Photo Source: TechInsights







EUV effect on # spacers will be limited as 193i → EUV + SDDP

PEALD PROCESSES FOR LOGIC APPLICATIONS

M0: Co with TiN/WC liner

SiC SiN VCT

TechInsights

M0

Fin

M0

SAC VCT

SAC VCG

Metal Gate

SD

SiGe Fin

Capping layers

Contact liners

Gate spacers

Gate fill

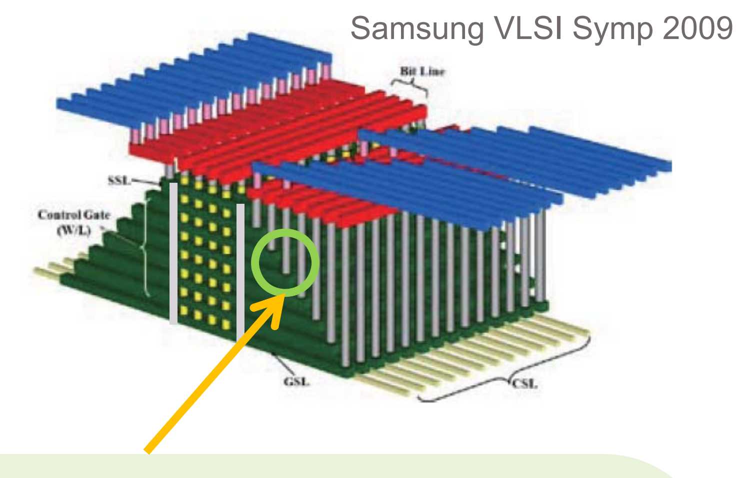
IO gate oxides

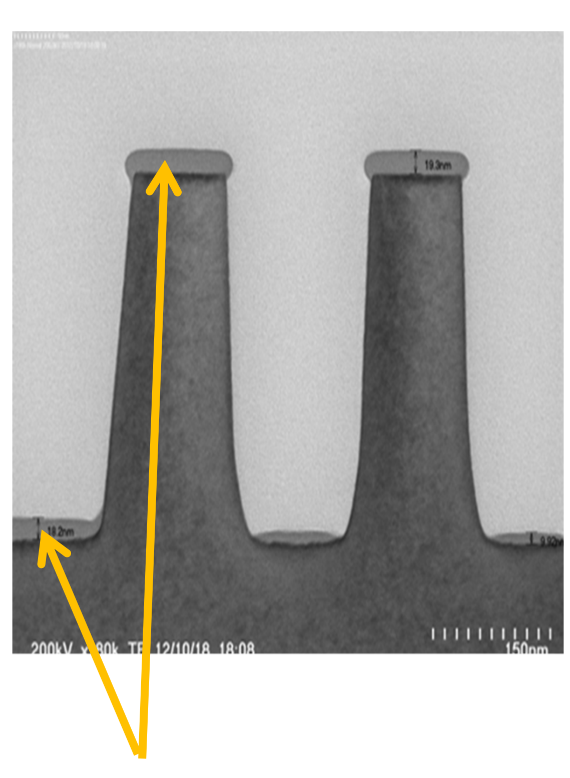
STI liners

Leading edge logic devices are using PEALD for many layers, because of the requirement of low thermal budget by using SiGe channel and good conformality requirement for 3D structure.

PEALD SiN FOR 3D-NAND APPLICATIONS

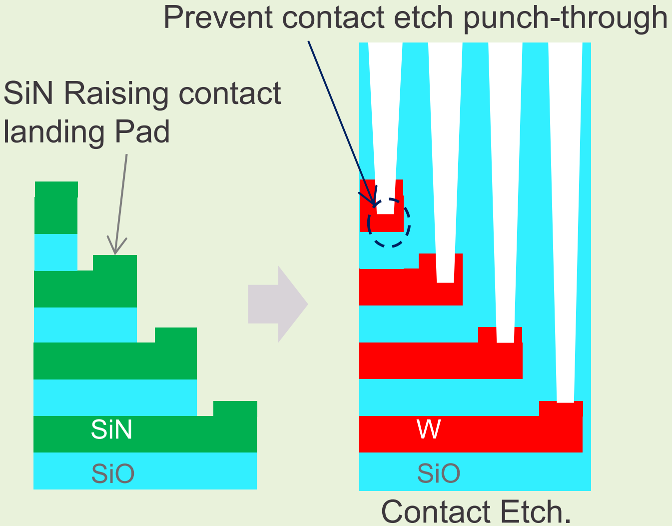
Samsung VLSI Symp 2009





- PEALD SiN

SiN film on Top and Bottom only

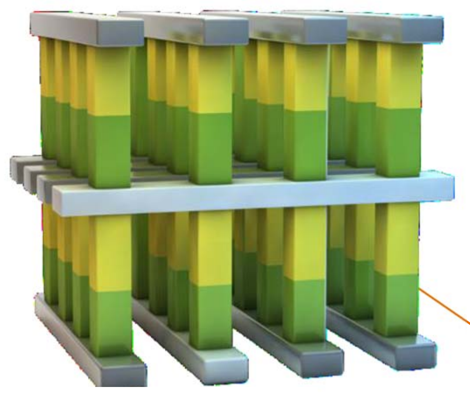


Fewer etch steps and more process latitude to create staircase

MEMORY HIERARCHY AND FUTURE TRENDS

- **DRAM and 3D-NAND scaling continues**
- **Many opportunities for new materials and ALD processes in new memories**

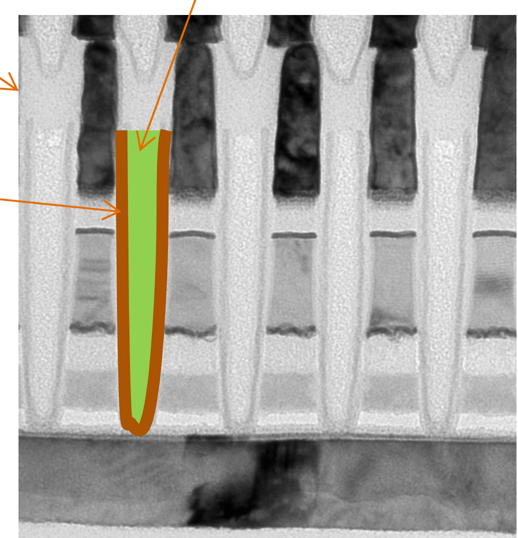
PEALD PROCESSES FOR 3D X-POINT



Source:Micron

- High Quality Low Temperature PEALD SiO2 Gapfill.
- Low thermal conductive material Gapfill for next generation.

- High Quality Low Temperature PEALD SiO2 liner



Source: TechInsights

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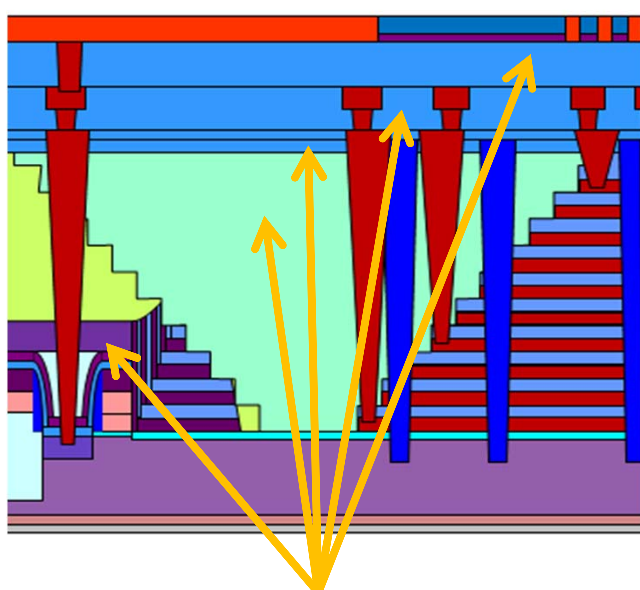
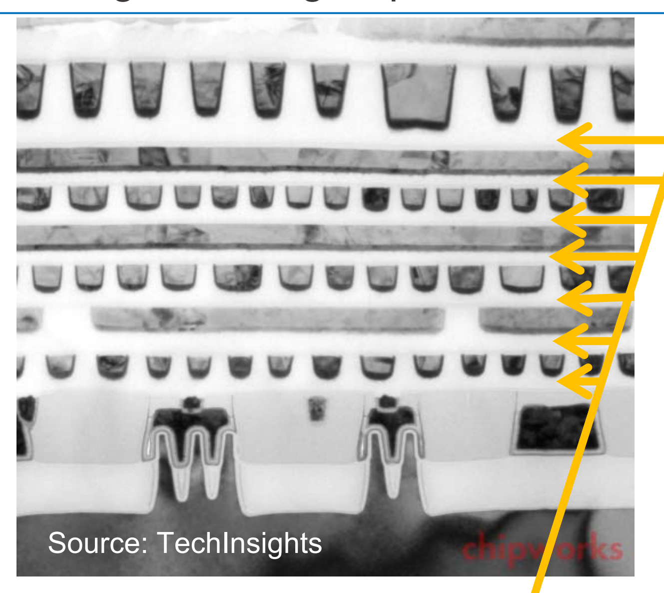
PECVD APPLICATIONS

3D-NAND



Logic and High Speed DRAM



TEOS
- High throughput
- Good wiw uniformity
- High quality
- Stress control

BEOL Low-k
- High throughput
- Good wiw uniformity
- Direct CMP
- No need for glue layer
- Stress control

Growing PECVD SAM in 3D-NAND, logic and CIS

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EPI PROCESS ROADMAP

Segment	Application	7nm	5nm	3nm
LOGIC	Channel – N Type	Undoped Si	Undoped Si	Undoped Si or HGAA
	Channel – P Type	Undoped Si	30% SiGe	30% SiGe or HGAA
	Source Drain – NSD	4% SiP	4-8% SiP / SiAs	>8% SiP / SiAs
	Source Drain – PSD	40% SiGe	>50% SiGe(B)	>50% SiGe(Ga)
	Source Drain – Preclean	Oxide Cln	Ox / Carbon Cln	Ox / Carbon Cln

Segment	Application	64 Stack	96 Stack	128 Stack
3DNAND	Memory Hole	SEG	SEG	SEG

Segment	Application	D1Z	D1A
DRAM	P Type Channel	30% SiGe	30% SiGe

Segment	Application	
ATM	EPI Wafer / Power Market	Atmospheric Deposited Doped / Undoped Films (~10μm – 100μm)

INTREPID ES: APPLICATION LIBRARY

LOGIC

Channel
- N-type
- P-type
- Si / SiGe HGAA

Source Drain
- NSD
- PSD

MEMORY

3D NAND
- Channel hole

DRAM
- Storage node contact

9 nm Si
11 nm $Si_{0.60}Ge_{0.40}$
10 nm Si
11 nm $Si_{0.60}Ge_{0.40}$
Depth (nm)
20 nm

SiGe / Si gate
all around device
Source: imec

100 nm

Si nanowire:
8nm radius
Source: imec

eSiGe:B (~60% Ge) (PM3)
W05
3% eSi:P

Excellent uniformity,
SiP (3% P)
Source: imec

4-Fin resistance (Ω/µm)

Contact resistivity (Ω cm)

ASM-imec SiP

A library of applications are available on the Intrepid ES

INTREPID ES: KEY FEATURES

- **Low Chamber Volume**
- **Dual Temperature Measurement: Pyrometer / TC**
- **Isothermal Quartz Chamber: Closed Loop Control**
- **Production Proven with High Productivity**

Intrepid ES delivers *isothermal* process modules for improved within wafer and wafer-to-wafer performance with the highest throughput

TRENDS IN EPITAXY: ASM SOLUTIONS

Epi Trends	ASM Solutions
Logic: 1) Doped Films for S/D Technology Extension 2) GAA → stack layers with precise interface control (Si / SiGe)	Low chamber volume produces predictable laminar gas flow over the wafer for precise doped film control and film interface transitions
Low temp. processing	TC control (pyrometry limitations <550°C) + isothermal kit Higher GR achievable due to better precursor utilization and lower dilution
Memory: 3D NAND → low cost / high throughput	Isothermal kit with multi-wafer clean
Pre-clean Chamber Evolution	SiO_2 + $SiGeO_x$ and interfacial carbon removal (Epi platform integrated with Previum pre-clean)

ASM continues to develop innovations to address Epi technology trends

INTREPID ES: STABLE FILM PROPERTIES WITH ISOTHERMAL QUARTZ CHAMBER

Center Thickness

Center P%

Ave. Thickness

Ave. Phosphorus%

Data Summary

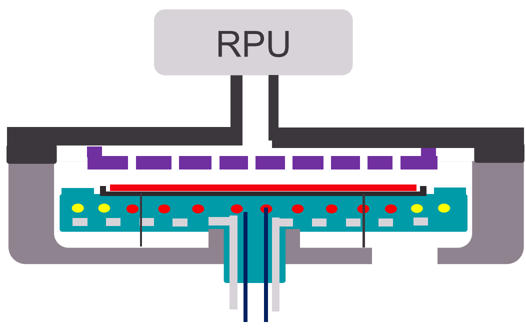
	Ave. THK (A)	Center THK (A)	Ave. P%	Center P%
Mean	529.3	525.4	4.13	4.02
Min	519.8	518.9	4.10	3.98
Max	539.4	533.3	4.18	4.07
Range	19.5	14.4	0.08	0.09
NU% (max-min) / 2 * Ave	1.8	1.3	1.0	1.1

Chamber clean after 1,200 wafer cycles

Intrepid ES: No Thickness Drift with Isothermal Quartz Chamber Control

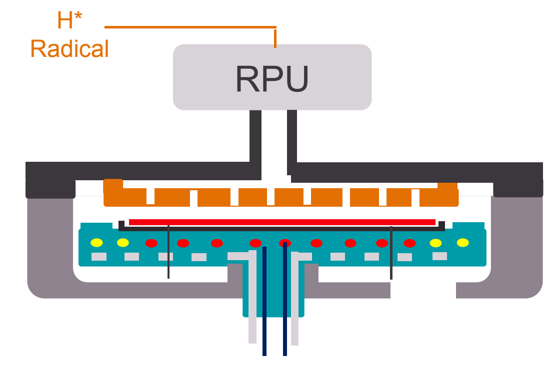
PREVIUM: INTEGRATED SURFACE PRE-CLEAN FOR ADVANCED LOGIC APPLICATIONS

Previum

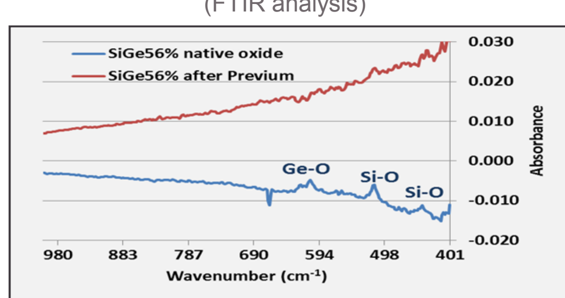


- ✓ In-situ conversion / sublimation for SiO_2

Previum Next for C Removal



$Si_{0.44}Ge_{0.56}$ oxide removal in Previum (FTIR analysis)



Optimized pre-clean process to remove $SiGeO_x$

- ✓ In-situ conversion / sublimation for SiO_2 AND $SiGeO_x$
- ✓ H* radical for carbon removal
- ✓ Leveraging ASM strength in high temp. chamber technology

Previum pre-clean chambers used with Intrepid ES Epi chambers for advanced logic development

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ASM PRODUCTS
FURNACE CVD /DIFFUSION /BATCH ALD

› A412 PLUS

- Dual boat/dual reactor system
- Clustering of different applications between reactors possible – only vertical furnace in the market with this capability
- Up to 150 product wafer load size

› A400 for More than Moore Devices

- Dual boat/dual reactor system
- Simultaneous handling of Dual size wafers
- Up to 150 product wafer load size

› Applications:

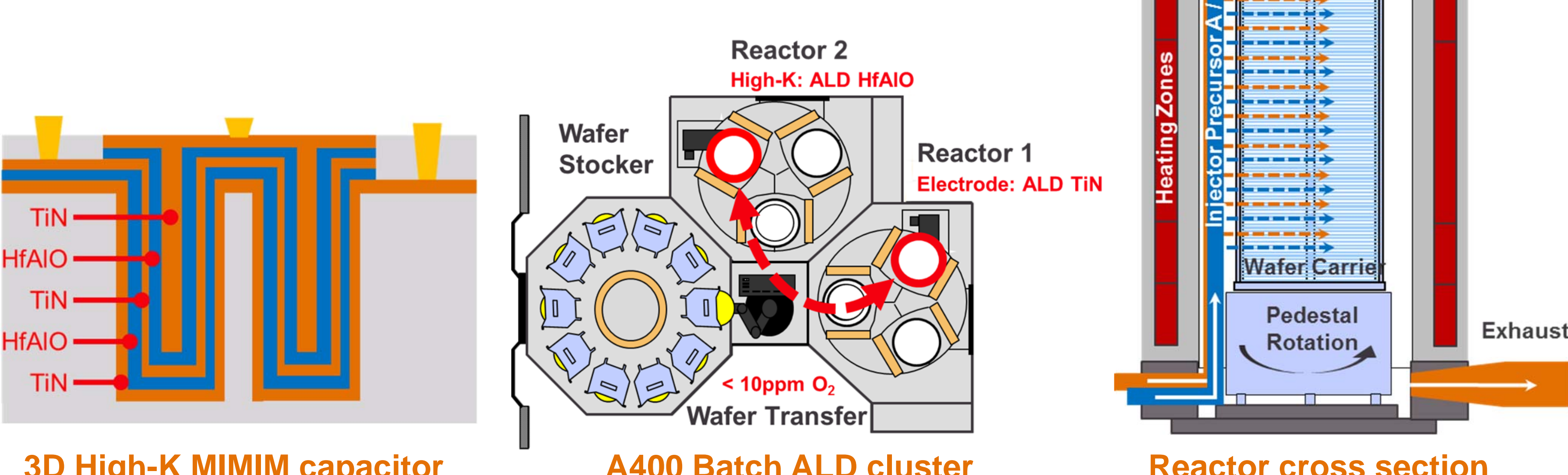
- Full range of applications for Logic, Memory, Power and MEMS Devices

- LPCVD Silicon, SiN, TEOS, HTO
- Diffusion, Anneal, Cure, Reactive Cure
- Batch ALD (AlO, AlN, TiN, SiN, SiO, etc)

A400 / A412 FURNACE - INNOVATION

Example: Dual reactor batch ALD cluster for IPD 3D High-K capacitors

- Integrated Passive Devices consist of inductors, resistors and capacitors embedded in a Silicon Interposer or Wafer Level Package
- This technology enables further IC miniaturization, lower cost and high-value precision which is driven by the Application Processor and Mixed Signal markets
- High capacitive density is achieved through deep trench 3D High-K MIMIM capacitors made by conformal ALD processes
- ASM has leveraged the dual reactor furnace concept to integrate both Metal Electrode and High-K materials in a high yield Batch ALD cluster solution



3D High-K MIMIM capacitor

A400 Batch ALD cluster

Reactor cross section

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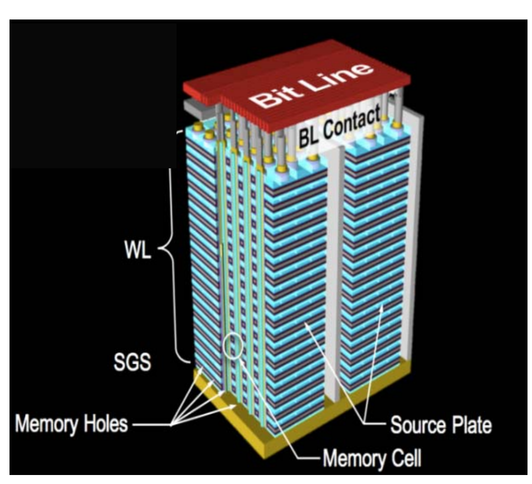
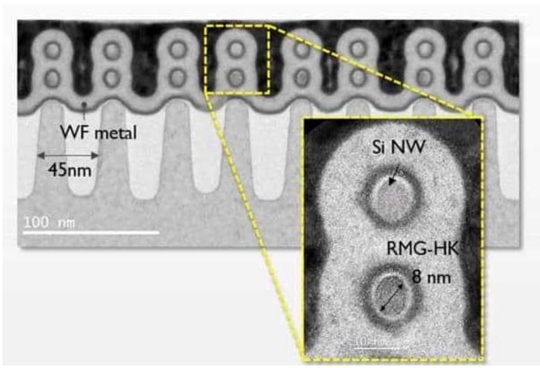
DEVICE STRUCTURE EFFECT ON ALD TECHNOLOGY

ASM

ALD= Plasma ALD (PE ALD) + thermal ALD

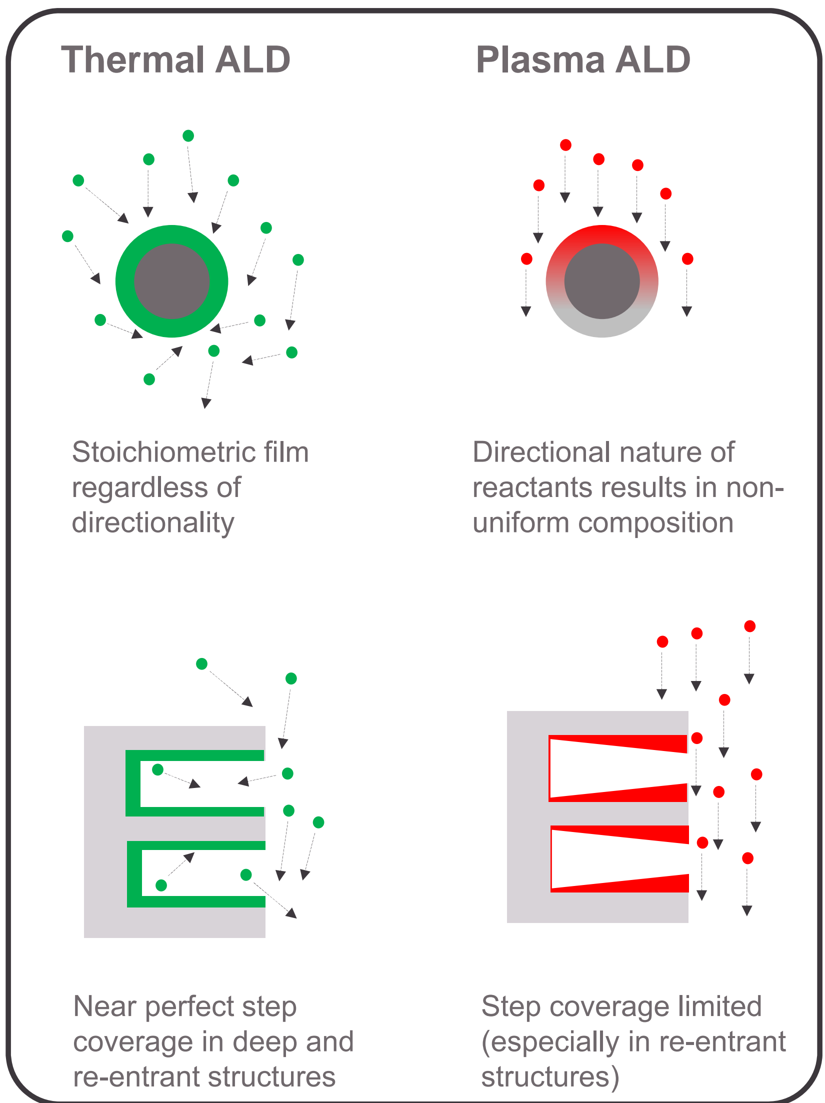


Source: Semiconductor Engineering



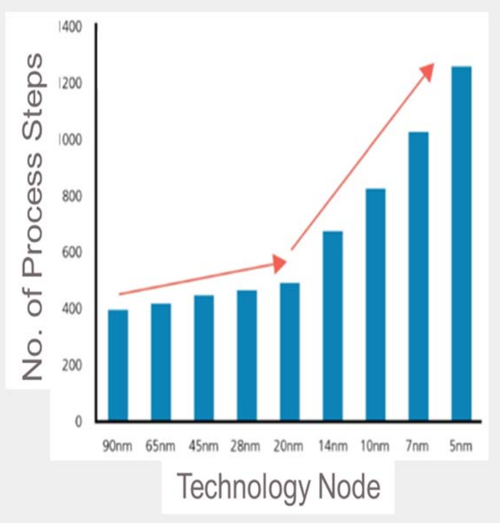
Source: IMEC

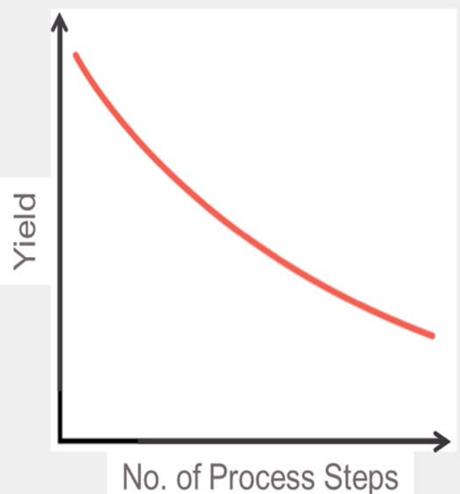
› **Move to 3D devices necessitates the use of pure thermal ALD techniques**



INTRODUCTION

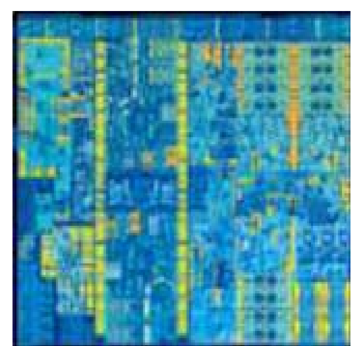
- Vertical processing (3DNAND, FINFET, GAA) has added a need for non-directional deposition processes (conformal and selective), which drives increased usage of *thermal* processes
- Continued shrinking gave rise to thicknesses as low as 3Å and thickness uniformity control of 0.1Å!
- Continued trend to lower temperature processing has resulted in *tighter* hardware component control
- The culmination of vertical processing, thinner films and lower temperature makes ALD *equipment strategies* for enabling higher process yield extremely important





HOWEVER, COSTS ARE ESCALATING AS WELL…

- Cost of high end fabs are escalating due to cost of equipment (EUV, multiple patterning, novel metrology, etc…)



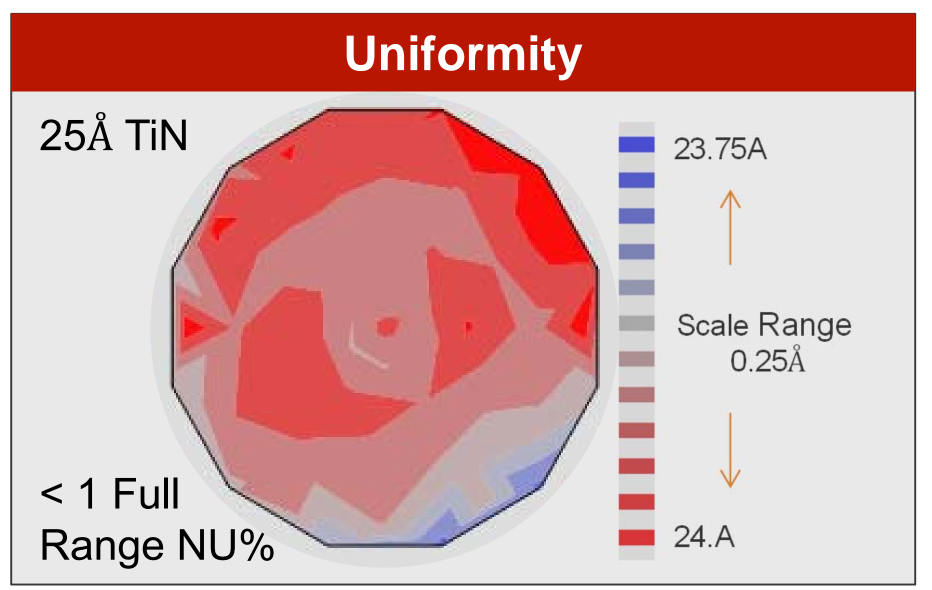
Intel 10nm Cannon Lake Chip
>10B transistors at cost of
<0.00001 cent per transistor

Source: Intel

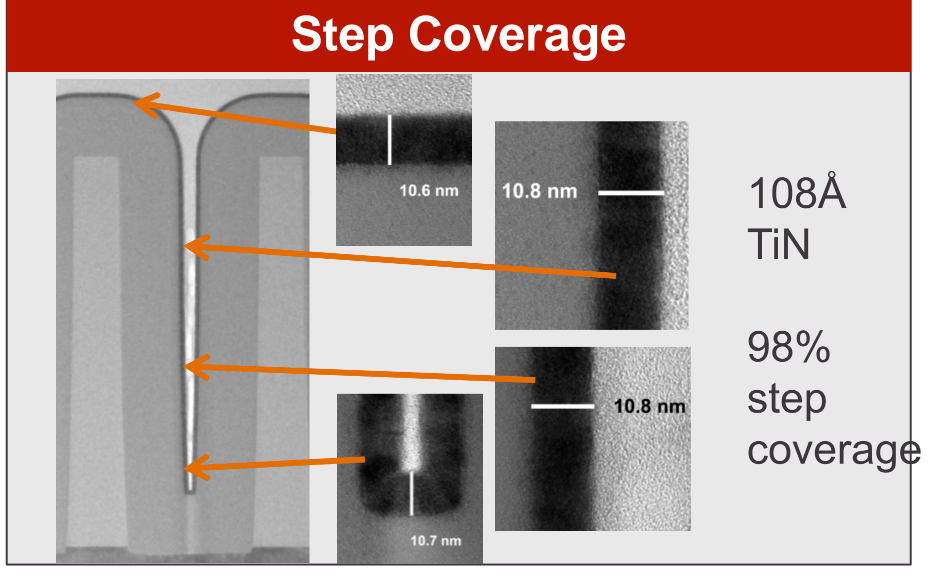
ALD needs to provide the atomic level control at competitive cost

ALD - ENABLER OF NEW MATERIALS
- KEY STRENGTHS OF ALD

Uniformity



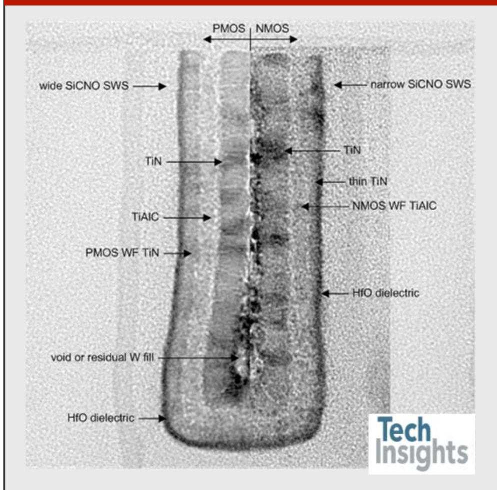
Step Coverage



108Å TiN

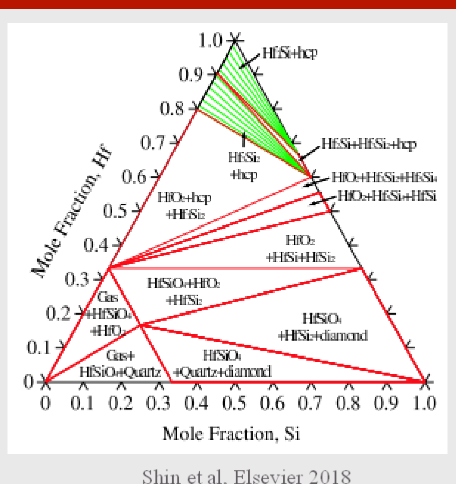
98% step coverage

Interface Control



Atomically engineered interfaces to optimize leakage current, reliability and work-functions

Composition Control



Shin et al, Elsevier 2018

Excellent composition control for ternary alloys e.g all ALD HfSiO solution demonstrated for DRAM peri gate oxides

GROWTH OF ALD IN SEMI INDUSTRY - ALD THE NEW CVD

2003

3-4 layers
ALD Al_2O_3, ZrO_2

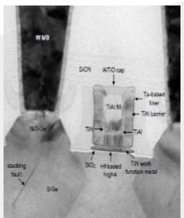
Infineon NOLA DRAM
www.future-fab.com

DRAM HSG structures
ASM

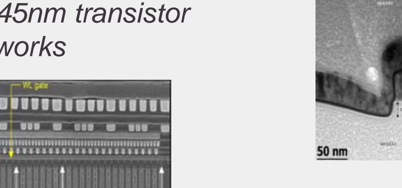
DRAM MIM Capacitor

2008

10+ layers
ALD HfO_2, ZrO_2
ALD TiN, TaN



Intel 45nm transistor
Chipworks

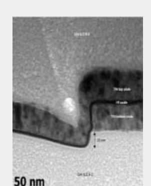


IBM FEOL eDRAM
Chipworks

+ Logic HKMG
+ FEOL eDRAM MIM

2013

20+ layers
ALD HfO_2, ZrO_2, ZAZ, SiO_2, SiN, PSG, BSG…
ALD TiC, TiN, TaN,



Samsung 30nm SDRAM
Chipworks

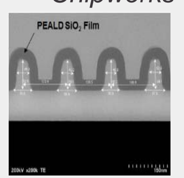
+ Patterning Materials
….

2018

50+ layers
ALD HfO_2, ZrO_2, ZAZ, SiO_2, PSG, BSG, SiN, Al2O3…
ALD TiC, TiN, TaN, Co, FFW, Mo, HfAlO, ZrAlO, YSiO, ...

Intel 22nm FinFET transistor
Chipworks

Intel 22nm BEOL capacitors
Chipworks

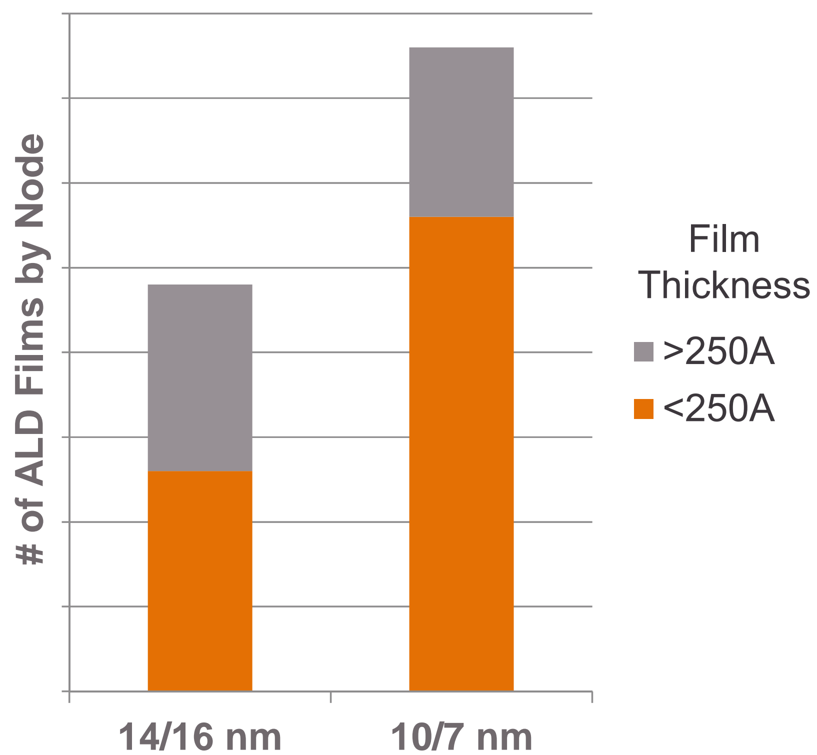


PEALD SDDP on Resist
ASM

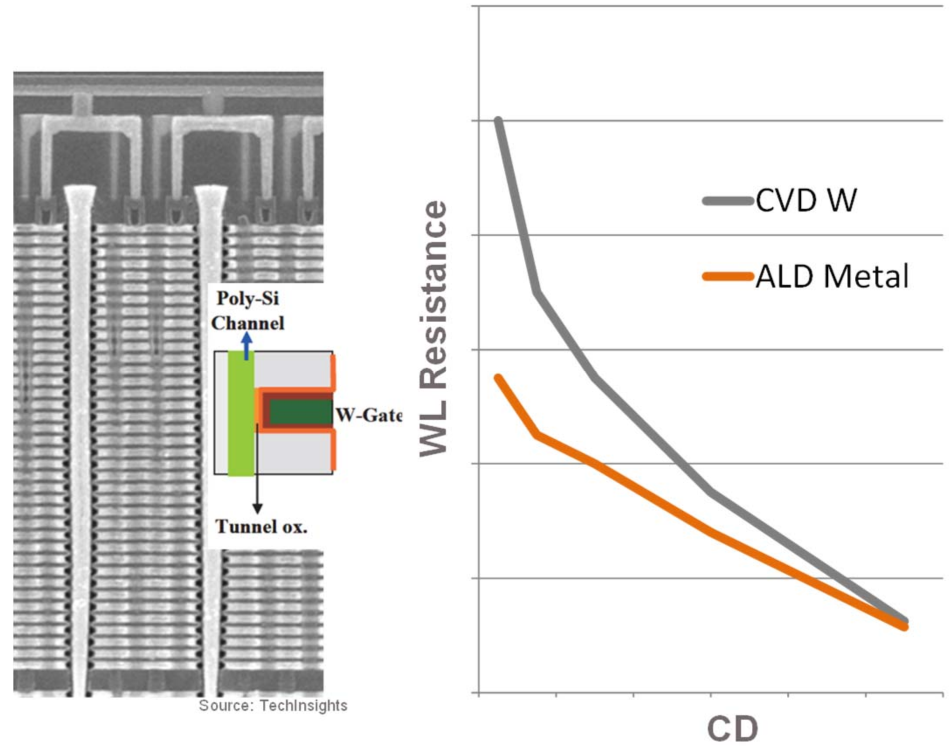
+ ALD Metal
+ ternary metal oxides
….

INCREASING USE OF ALD FILMS

CHIP DENSITY DRIVING THIN PATTERNING FILMS



CHALLENGES IN METAL SCALING IN DRAM AND 3DNAND TECHNOLOGY



Largest area of growth is in thinner films - ESL and HM films in high demand

Thermal ALD technology delivers high performance pure metal solutions

INTRODUCING SYNERGIS® ALD

- New dual chamber thermal ALD reactor technology evolved from decades of **ALD expertise** on Pulsar and EmerALD

- Leverages industry proven XP8 platform architecture for **high productivity** solutions for logic and memory applications while maintaining **single wafer process control**

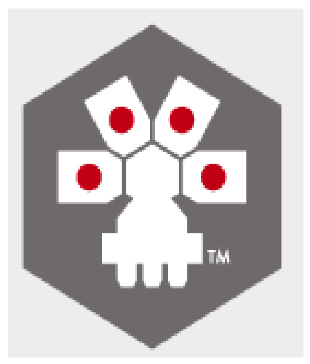
- Highly **flexible** source layout including ASM's proven **solid source delivery** technology

- Ability to run clustered processes with **high tool availability** to lower overall cost per wafer

EmerALD Pulsar Synergis

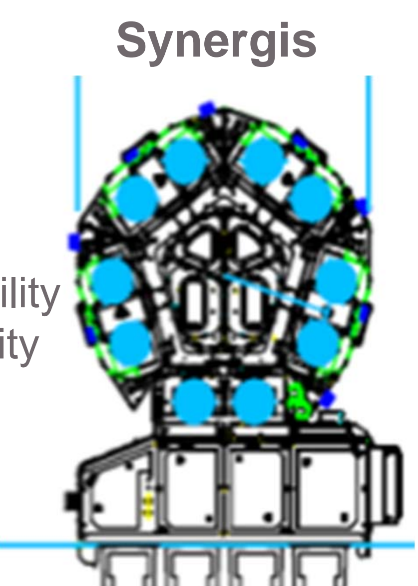
SYNERGIS® COMBINES KEY ALD TECHNOLOGIES

Single Wafer



Clustering
Process Flexibility
High Productivity

Synergis



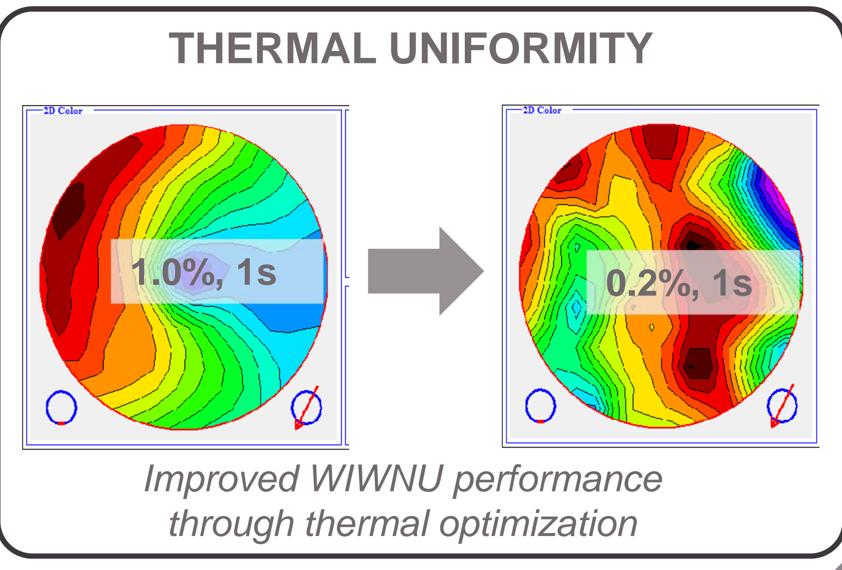
Synergis®

› **Designed to advance performance of industry ALD toolsets:**

1. **Improve wafer thermal uniformity**
2. **Enable delivery of low vapor pressure precursors & added process flexibility**
3. **Manufacturability – Short PM Time & High Throughput**
4. **Reduce reactor volume and improve purge efficiency**

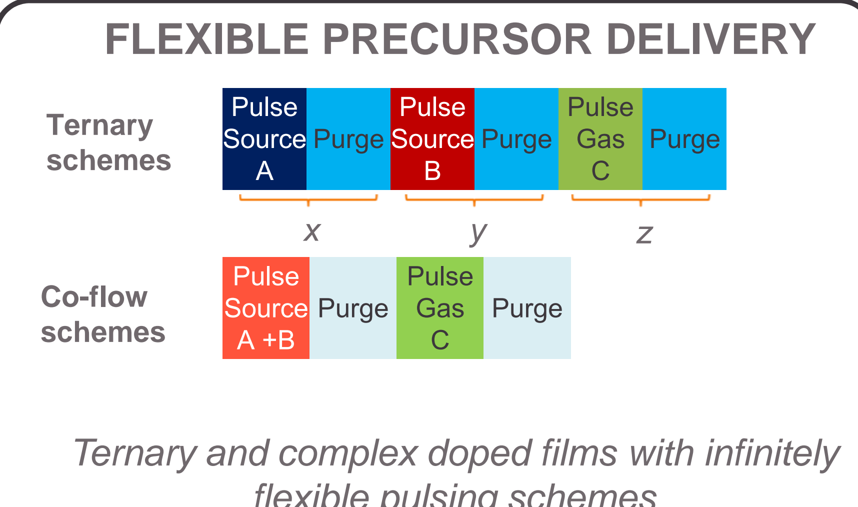
SYNERGIS® INNOVATIONS FOR FLEXIBILITY AND PERFORMANCE

THERMAL UNIFORMITY



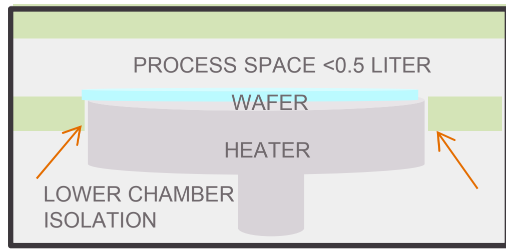
Improved WIWNU performance through thermal optimization

FLEXIBLE PRECURSOR DELIVERY



Ternary and complex doped films with infinitely flexible pulsing schemes

PURGE EFFICIENCY



True ALD performance with small reactor volume & high flow purge circuits

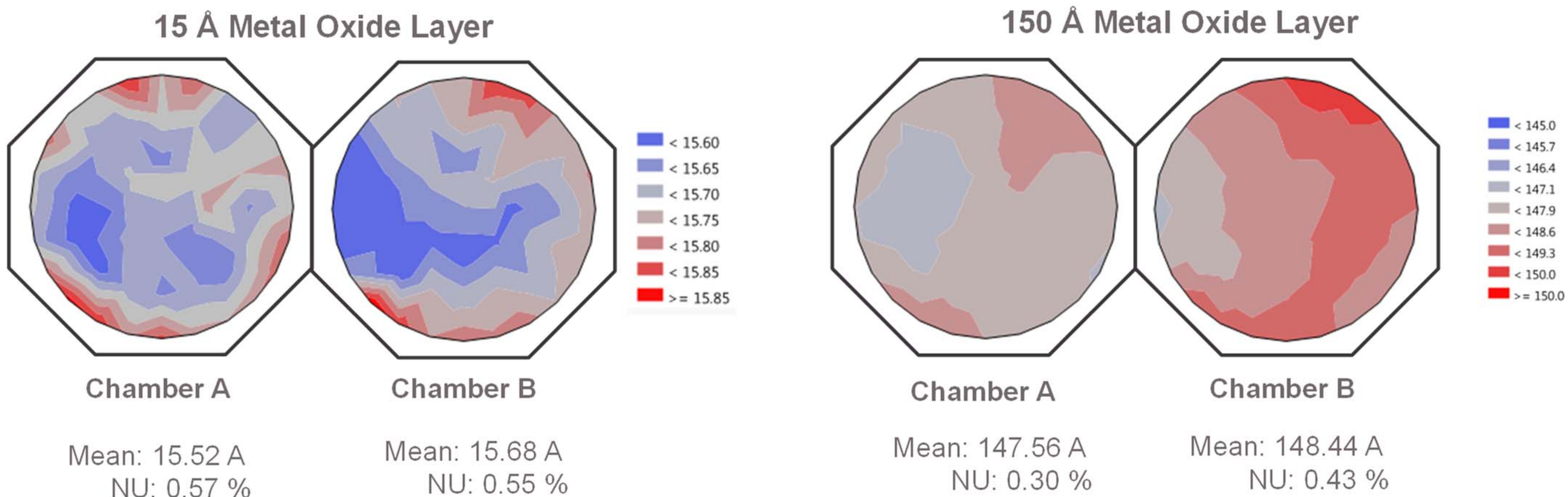
HIGH TOOL AVAILABILITY

Reactor in production

Reactor under maintenance

Reduced PM times with fast switch-out reactor packs

SYNERGIS® CHAMBER TO CHAMBER MATCHING



- **Unparalleled chamber to chamber matching for tight wafer to wafer control –irrespective of film thickness**

CONFORMAL TRUE ALD METAL DEPOSITION ENABLED BY SYNERGIS®

Top

Bot

Tech Insights

Entrance

Inner trench

Top

Top

Bot

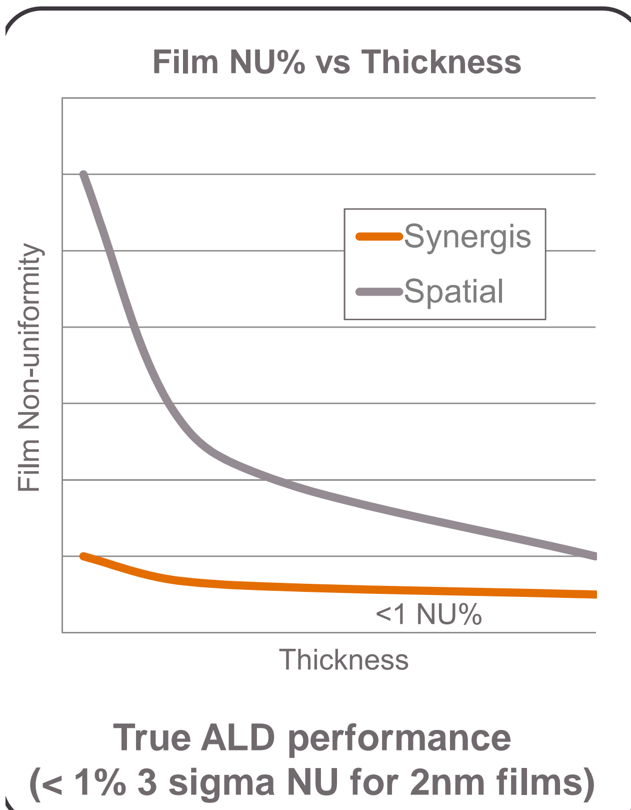
Bot

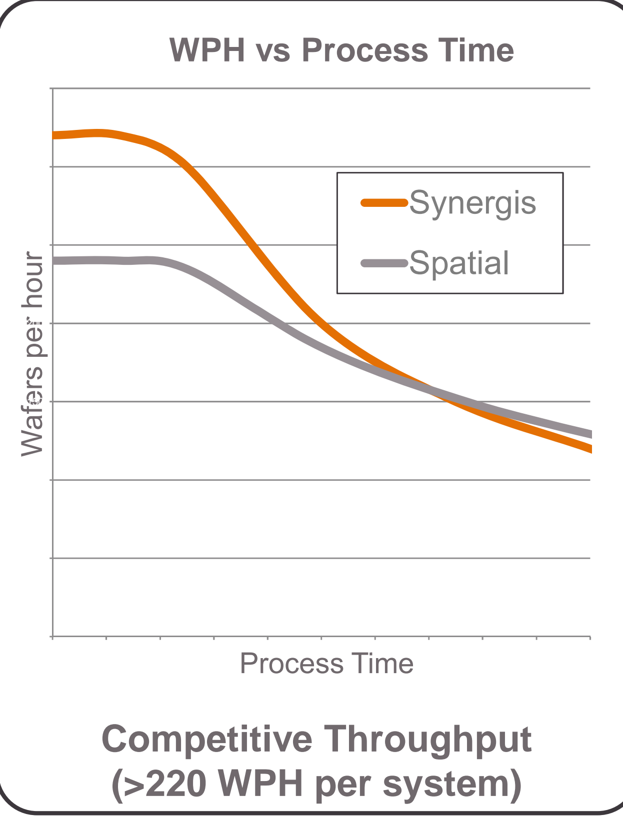
ASM Test Structures

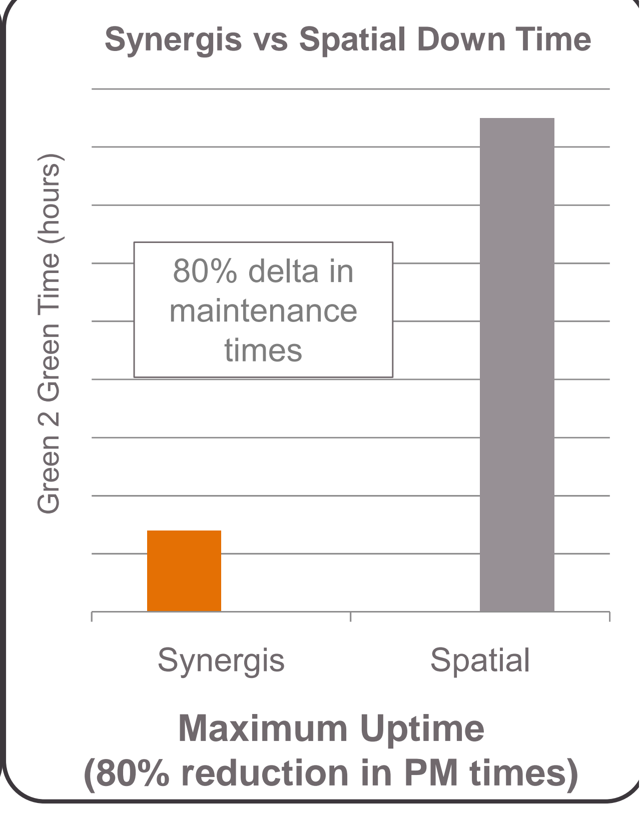
**Representative image*

- **Excellent step coverage of pure ALD metal demonstrated on 200X area-enhanced 3DNAND structures**

SYNERGIS® ENABLES ALD PRODUCTIVITY FOR THE EUV ERA







SYNERGIS® ADDRESSES THE EXPANDING ALD APPLICATION SPACE

DX: Low temperature, low-k encapsulation and hermetic sealing layers

MX: Metal oxide hard masks and etch stop layers with tunable etch properties

ML: Low resistivity pure metal layers for DRAM and 3DNAND word line

NT: Low resistivity, ultra-thin enhanced barrier solutions for logic and memory

SYNERGIS® ALD: HIGHEST PERFORMANCE AT THE LOWEST COST PER WAFER

- **Synergis® thermal ALD provides best productivity without sacrificing film performance**
  - Reduces cost per wafer for ALD technology by >60%
- **Flexible platform and architecture to meet needs of sub-7 nm technologies**
  - Ability to deposit metal oxides (MX), metal nitrides (NT), dielectrics (DX) and pure metals (ML)
- **Enables ALD SAM expansion to replace traditional CVD/PVD layers**