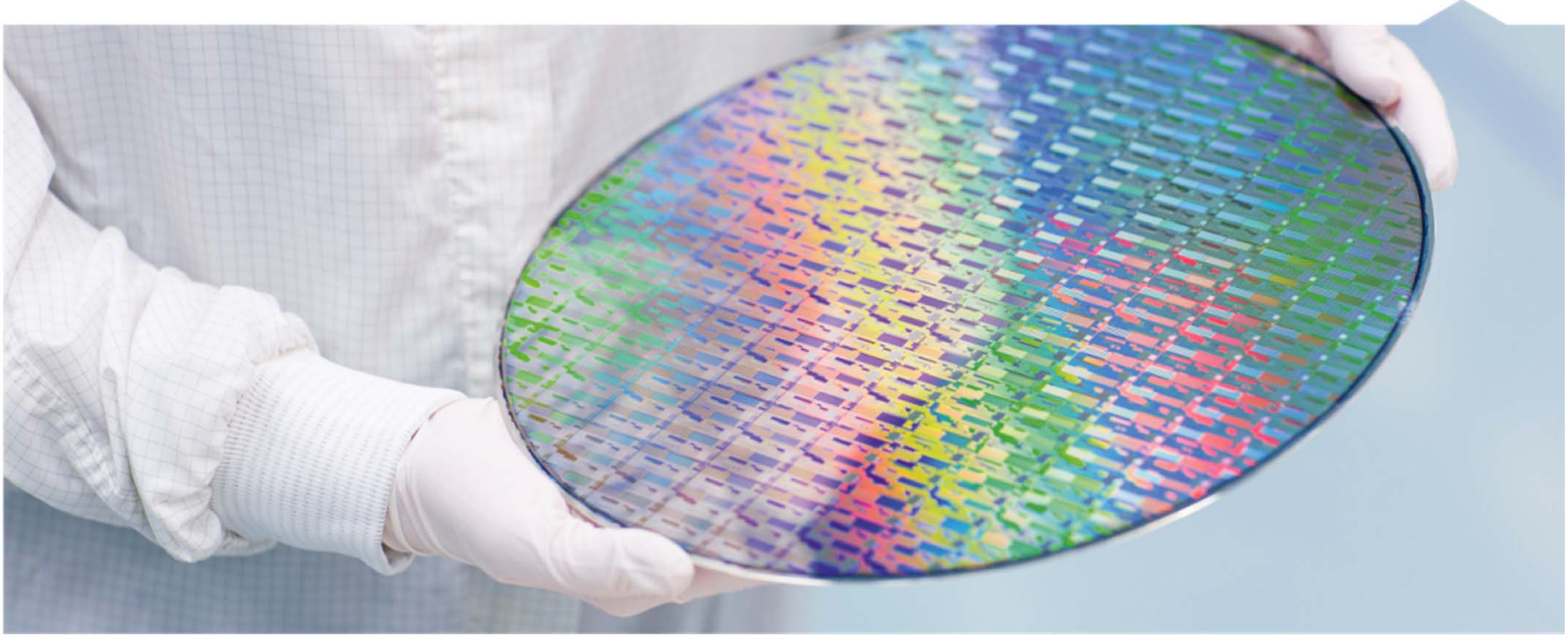
DRIVE INNOVATION · DELIVER EXCELLENCE >

ASM



ADVANCED CHIP MANUFACTURING WITH NEW MATERIALS

ASM International
Analyst and Investor Technology Seminar
Semicon West July 13, 2016

CAUTIONARY NOTE

Cautionary Note Regarding Forward-Looking Statements: All matters discussed in this press release, except for any historical data, are forward-looking statements. Forward-looking statements involve risks and uncertainties that could cause actual results to differ materially from those in the forward-looking statements. These include, but are not limited to, economic conditions and trends in the semiconductor industry generally and the timing of the industry cycles specifically, currency fluctuations, corporate transactions, financing and liquidity matters, the success of restructurings, the timing of significant orders, market acceptance of new products, competitive factors, litigation involving intellectual property, shareholders or other issues, commercial and economic disruption due to natural disasters, terrorist activity, armed conflict or political instability, epidemics and other risks indicated in the Company's reports and financial statements. The Company assumes no obligation nor intends to update or revise any forward-looking statements to reflect future developments or circumstances.

OUTLINE

- **Exponentials in the industry**
- **New Materials and 3D: Moore’s law enablers**
- **ASM and New Materials**
  - ALD as enabler of new materials
  - ASM New Materials development strategy
  - ALD supply chain components
- **ASM Products and selected applications**
- **Summary and Conclusions**

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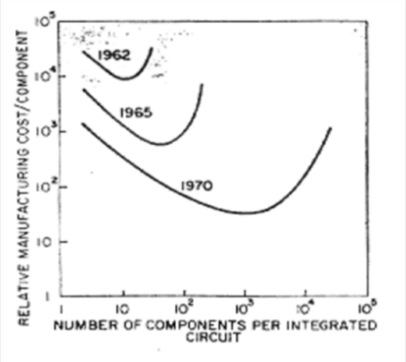
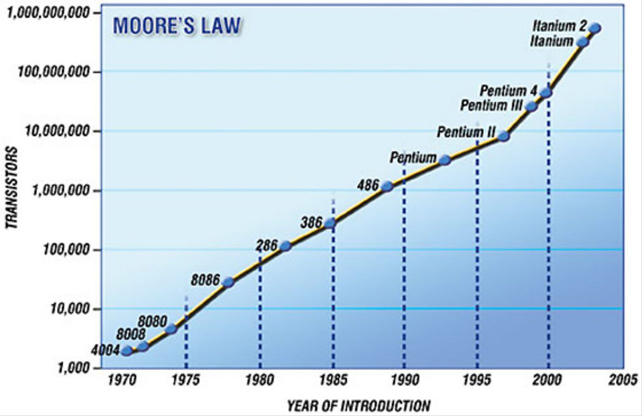
EXPONENTIALS IN THE INDUSTRY

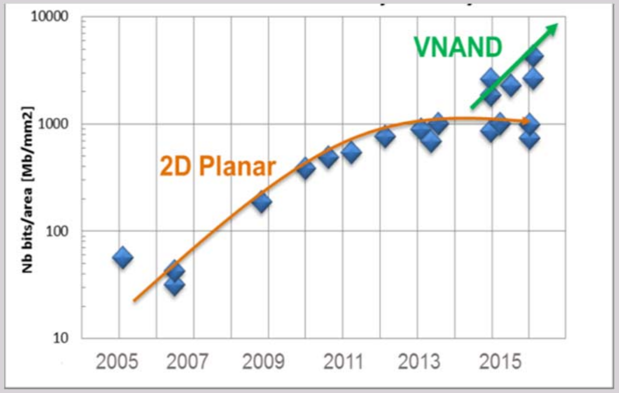
Moore’s Law



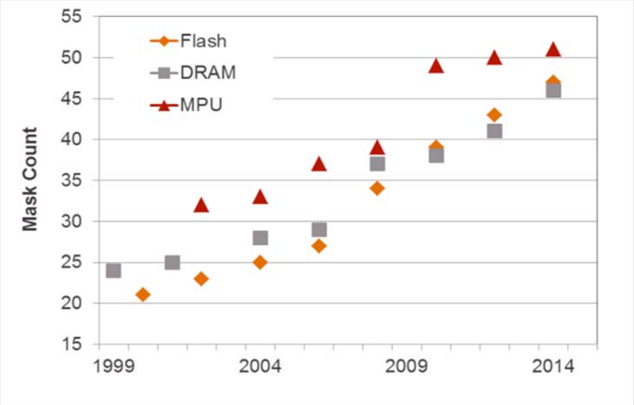
Density (xtor/chip)



Memory Density (Mb/mm^2)



Complexity (Mask Count)



Top: G. Moore, Electronics (1965); www.intel.com.
Bottom: ASM; Techinsights and ASM (2013);

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SCALING IS INCREASINGLY ENABLED BY NEW MATERIALS AND 3D TECHNOLOGIES

1990 1995 2000 2005 2010 2015 2020 2025

Scaling enabled by Litho

Patterning Spacers

Scaling enabled by Materials

Low-k

Strained Si

High-k

High-mobility Materials

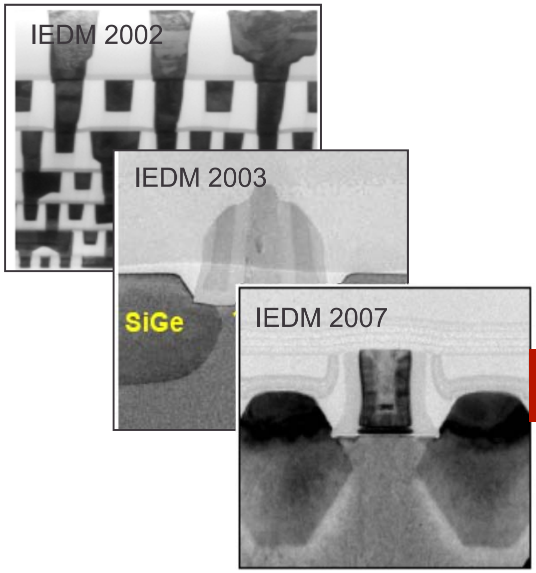
Scaling enabled by 3D

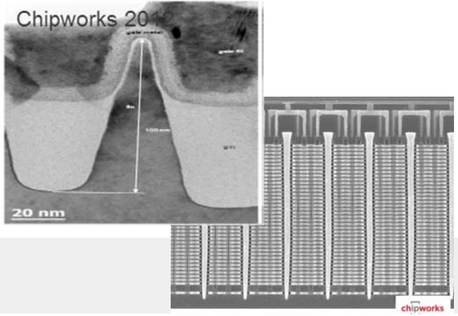
FinFET

3D TSV

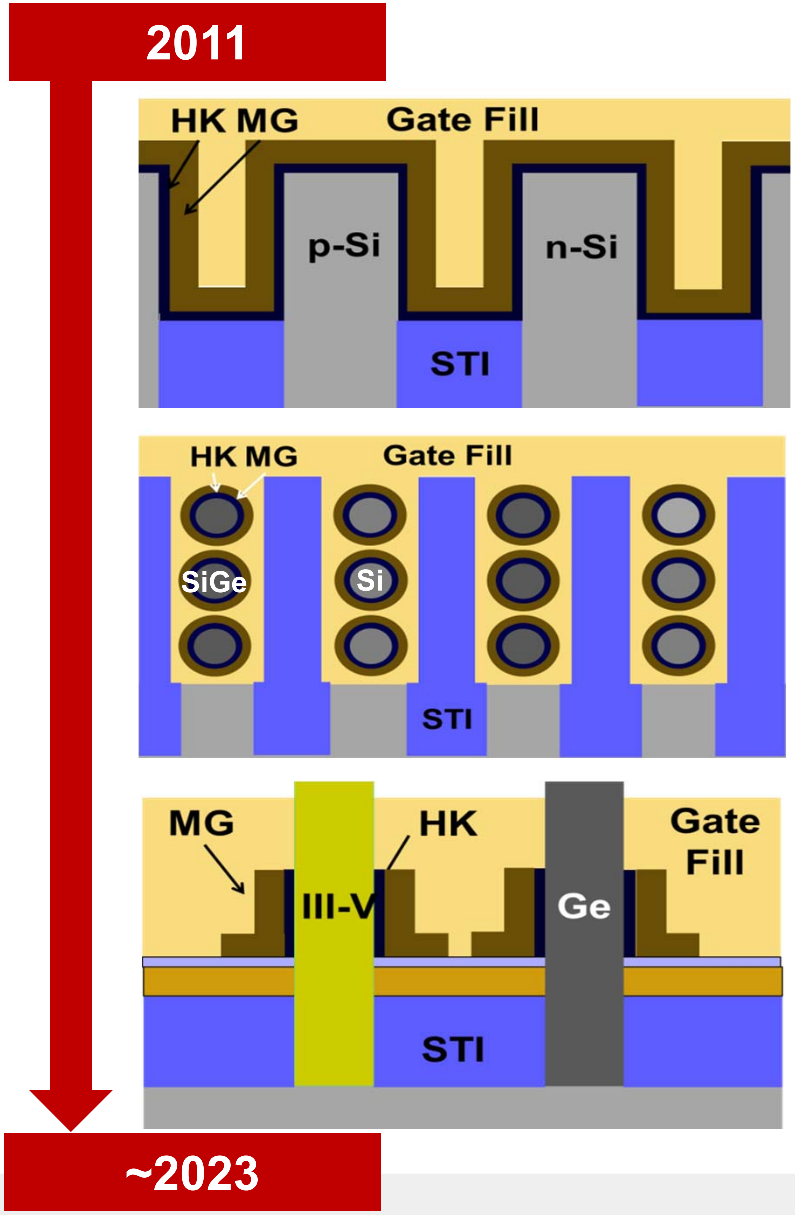
3D Memory

GAA





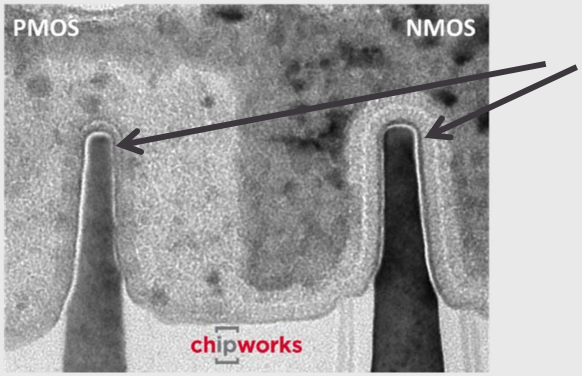
SCALING BY MATERIALS AND 3D



- Density scaling (continuing Moore’s law) driving towards higher mobility materials and alternate device architectures
- Future systems will integrate much wider variety of materials and device structures

NEW MATERIALS AND PROCESSES: MOORE'S LAW ENABLERS

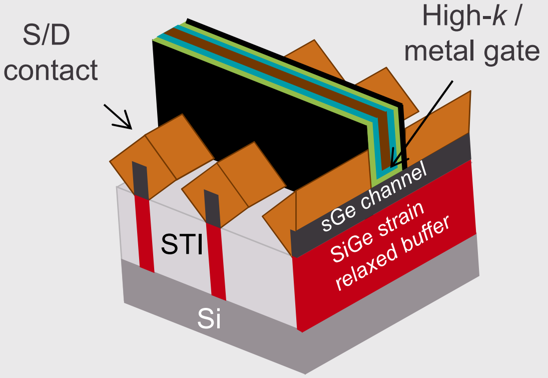
Higher Capacitance, Lower Leakage

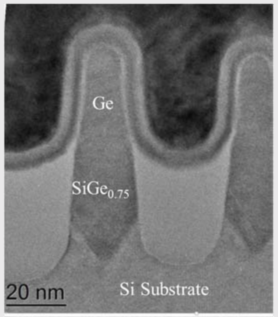


High-k / Metal Gate

DRAM, RF, decoupling capacitors

Higher Mobility, Lower Resistance

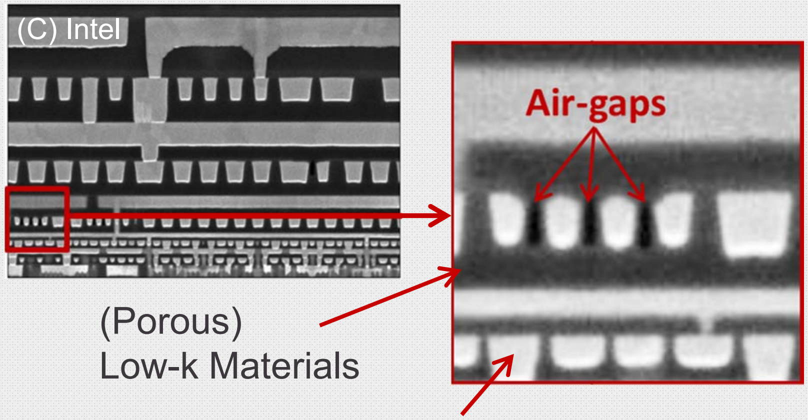




Mitard et al., VLSI '16

Strain and new Channel Materials
New metal contacts

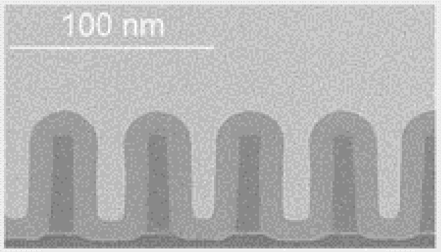
Less Cross Talk, Faster Interconnect



(Porous)
Low-k Materials

Improved Metals

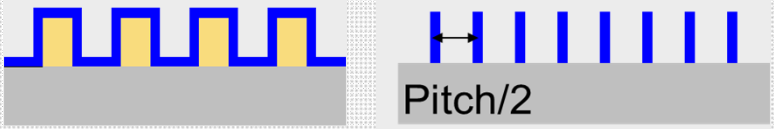
Smaller Feature Sizes



SDQP for
N7 and N5

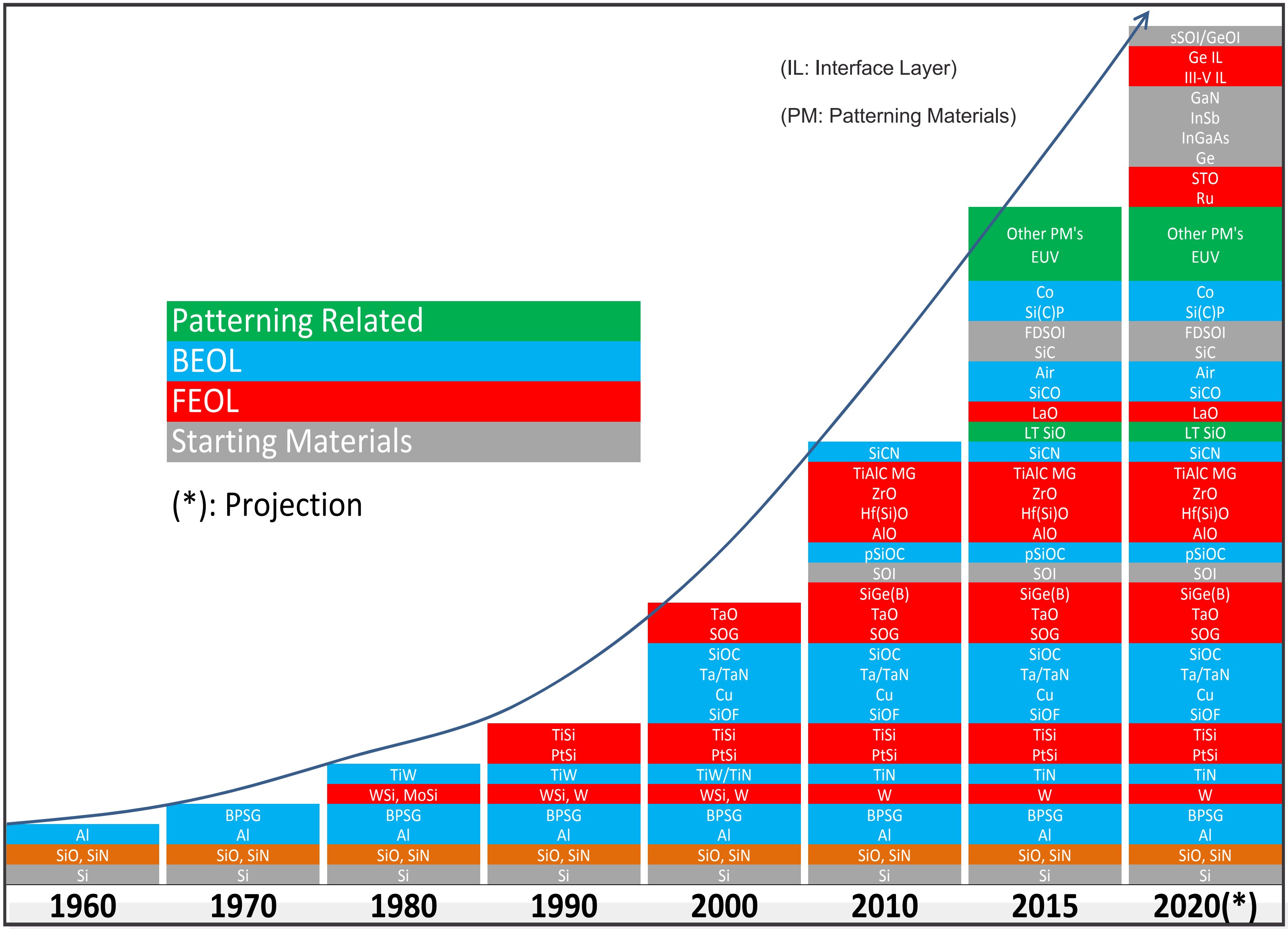
Conformal SiO_2

Anisotropic Etch



E. Altamirano-Sánchez et al., SPIE Newsroom, 14 May '16

NEW MATERIALS: MOORE’S LAW ENABLERS



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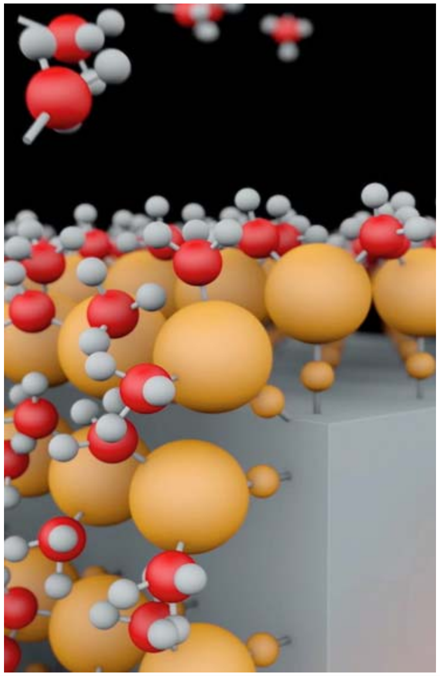
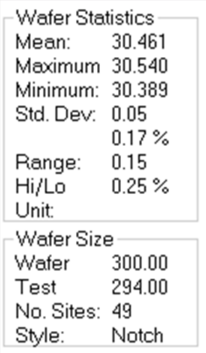
ASM AND NEW MATERIALS

- **ASM technology focuses on enabling new materials and new device integration roadmaps**
  - 3D transistor formation (FinFET & beyond FinFET)
  - DRAM, Flash –planar and 3D NAND - and emerging memory
  - More than Moore / IoT applications (MEMS, Sensors, Power)
- **ALD (Atomic Layer Deposition) separates reactive precursors in time (or space), and grows materials one “atomic” layer at a time**
  - Superb control of uniformity, quality, and composition
  - Conformal to any topography
- **Enabling high quality materials at lower temperatures**
  - high-k metal gates
  - low temp spacers for multi-patterning
  - Other emerging applications



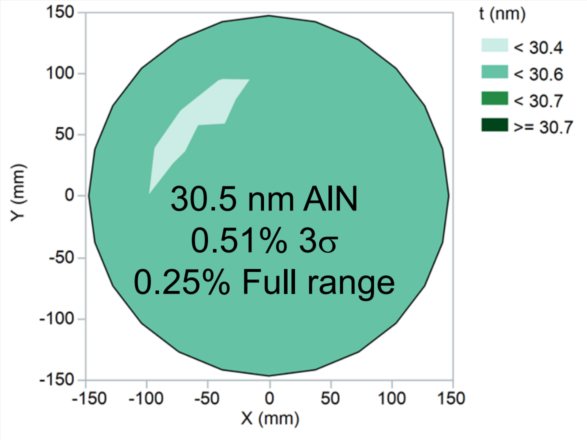
ALD AS ENABLER OF NEW MATERIALS - KEY STRENGTHS OF ALD

Uniformity



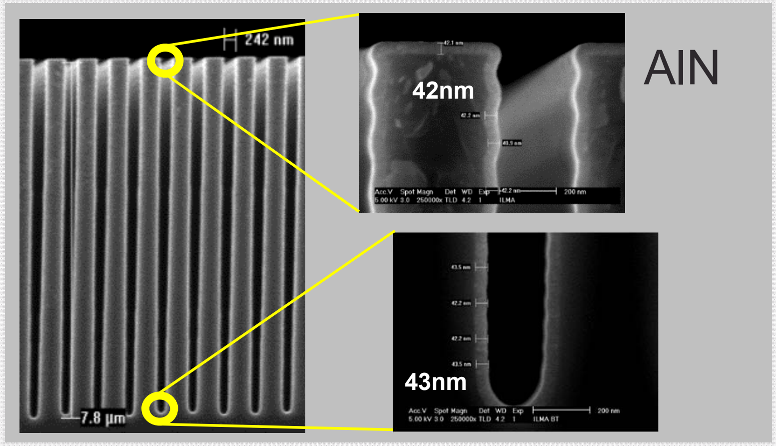
Wafer Statistics	
Mean:	30.461
Maximum	30.540
Minimum:	30.389
Std. Dev:	0.05
	0.17 %
Range:	0.15
Hi/Lo	0.25 %
Unit:	

Wafer Size	
Wafer	300.00
Test	294.00
No. Sites:	49
Style:	Notch



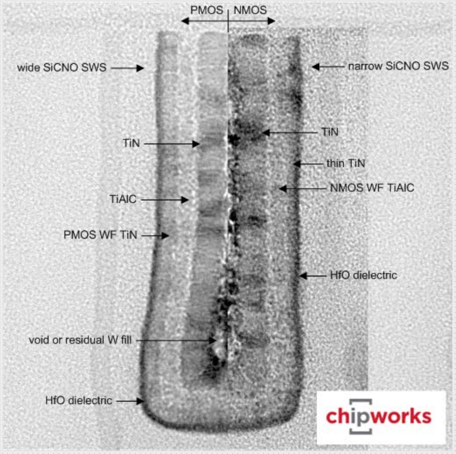
30.5 nm AlN
0.51% 3σ
0.25% Full range

Step Coverage



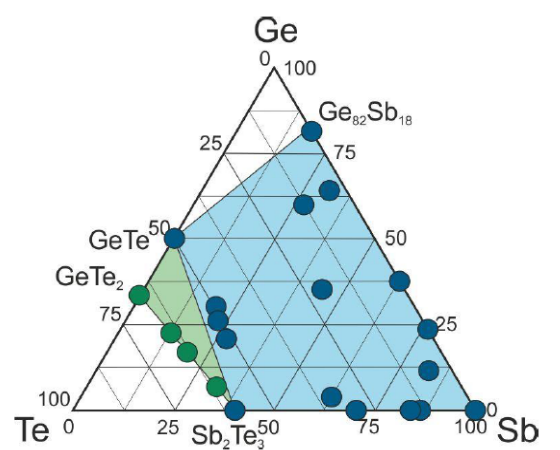
AlN

Interface Control



Atomically engineered interfaces to optimize leakage current, reliability and work-functions

Composition Control



Ritala, E/Pcos 2012;

Excellent composition control for ternary alloys; all ALD solution demonstrated for GST

CRITICAL ALD SUPPLY CHAIN COMPONENTS

Fundamental Capability

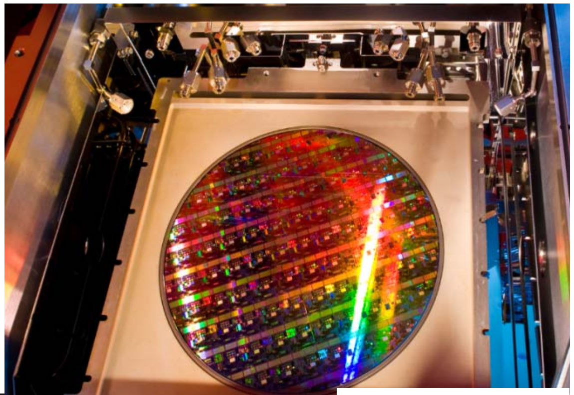
Process Performance

Productivity

Integrated Process

Final Product Capability


Pre-cursors


Reactors


High productivity tools


Pre-cursor Delivery, Valves and Vessels

Fab facilities, pumps & abatement

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ASM PRODUCTS
ALD

› **Pulsar® XP**

- ALD for high-k
- Cross-flow reactor
- Solid source delivery system

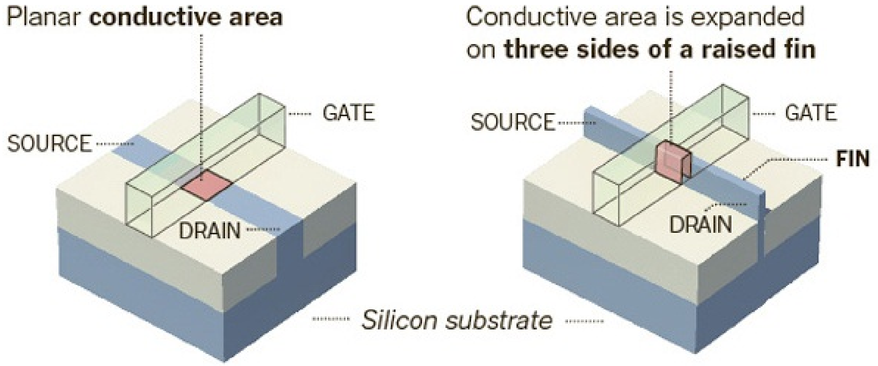
Pulsar® XP

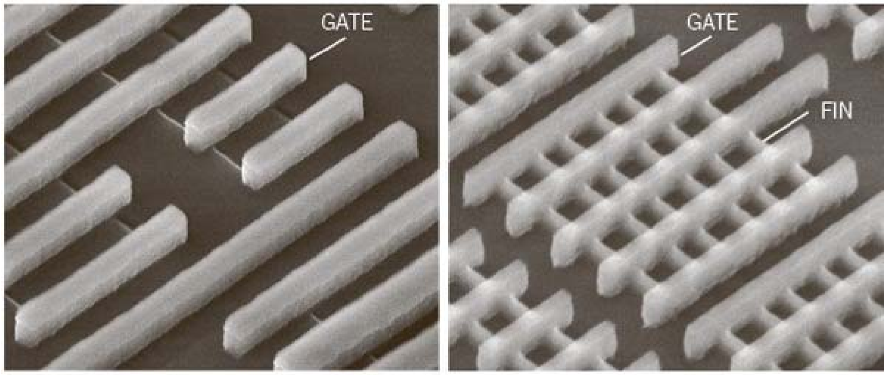
› **EmerALD® XP**

- ALD for metal gates
- Showerhead reactor

EmerALD® XP

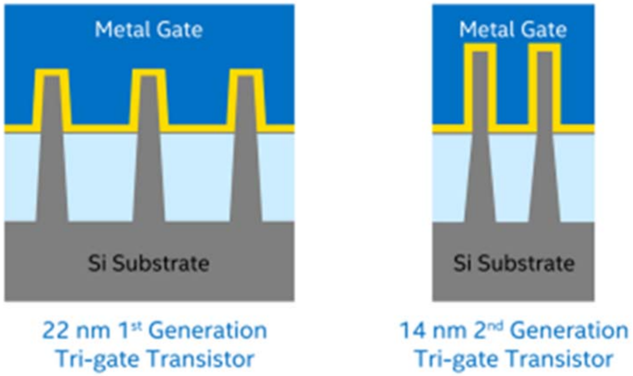
FINFET CHALLENGES:
ALD ENABLES FURTHER SCALING IN 3D





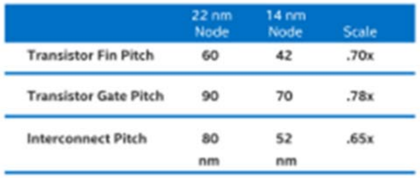
Source: Intel

THE NEW YORK TIMES



22 nm 1st Generation Tri-gate Transistor

14 nm 2nd Generation Tri-gate Transistor

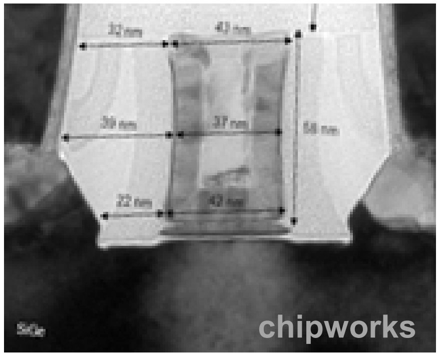


	22 nm Node	14 nm Node	Scale
Transistor Fin Pitch	60	42	.70x
Transistor Gate Pitch	90	70	.78x
Interconnect Pitch	80 nm	52 nm	.65x

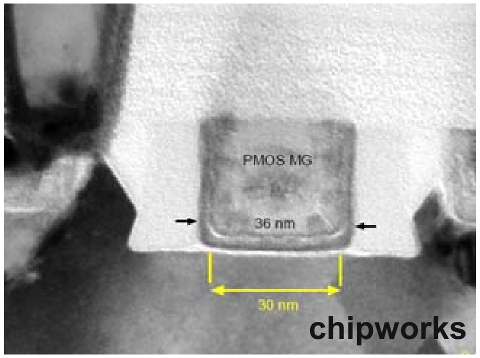
Source: Intel

- Materials properties and channel length must be uniform over fin height
- Conformal coverage required
- Aspect ratios increase going from 22nm to 14nm to 10nm
- → ALD technology has become critical for HK and MG layers

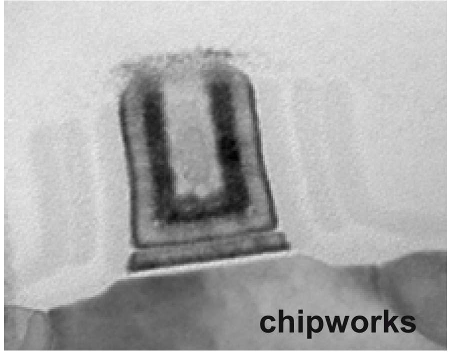
EXTENDIBILITY OF HAFNIUM BASED OXIDES



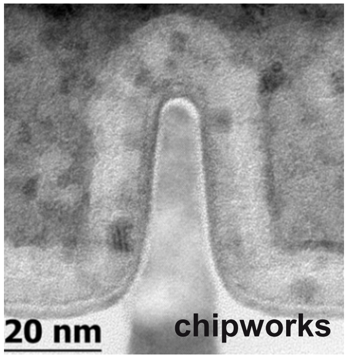
45nm HK first RPMG
Planar FET



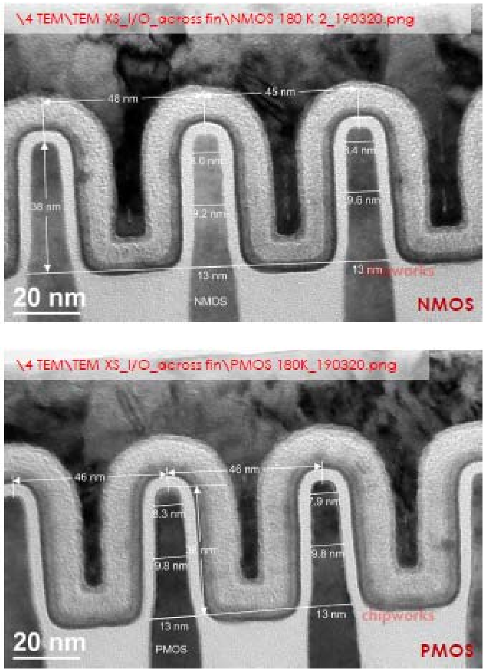
32 nm HK last RPMG
Planar FET



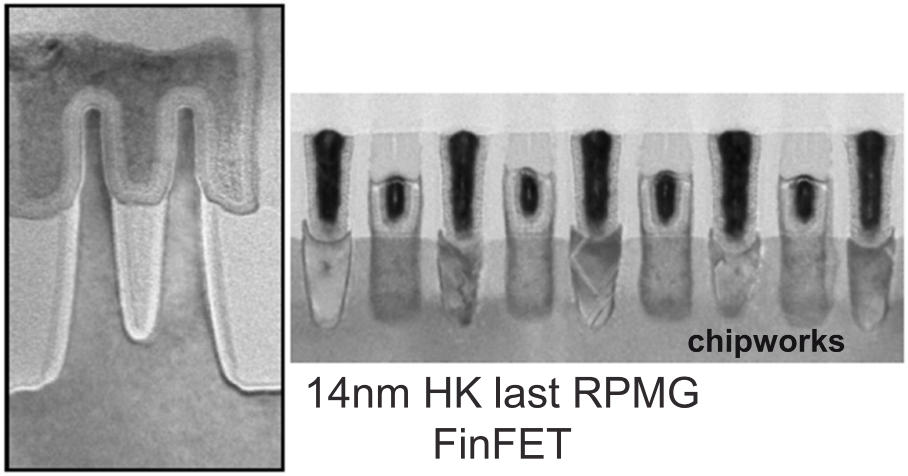
28nm HK first RPMG
Planar FET



22nm HK last RPMG
FinFET



16 nm HK last RPMG
FinFET

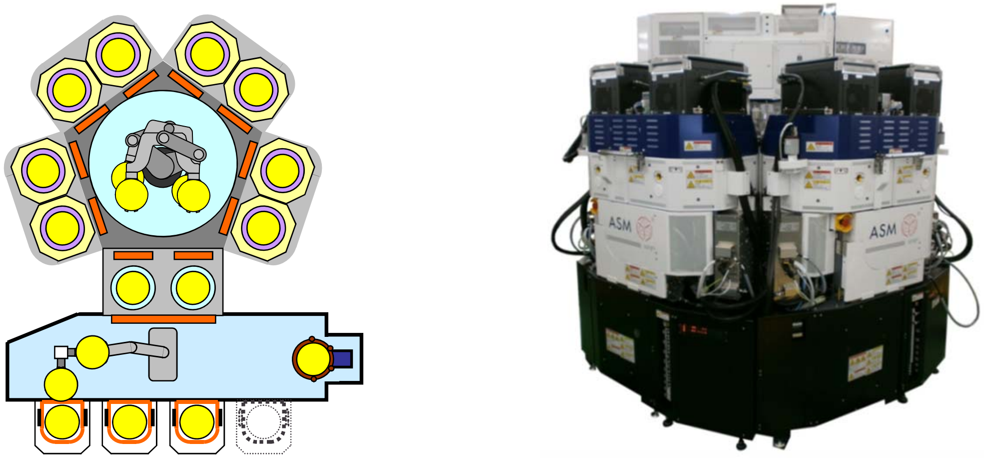


14nm HK last RPMG
FinFET

ASM PRODUCTS
PEALD AND PECVD

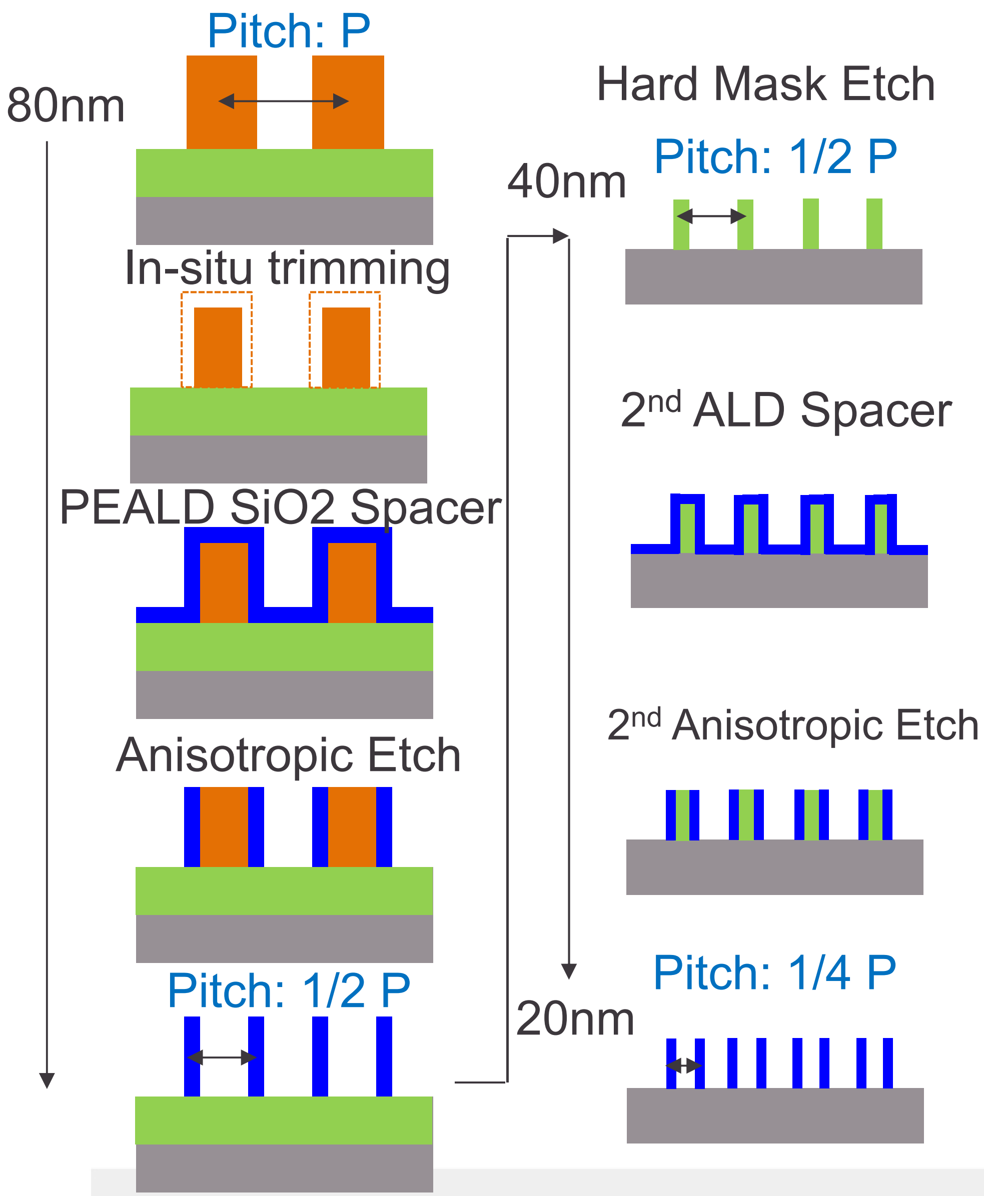
› XP8-DCM

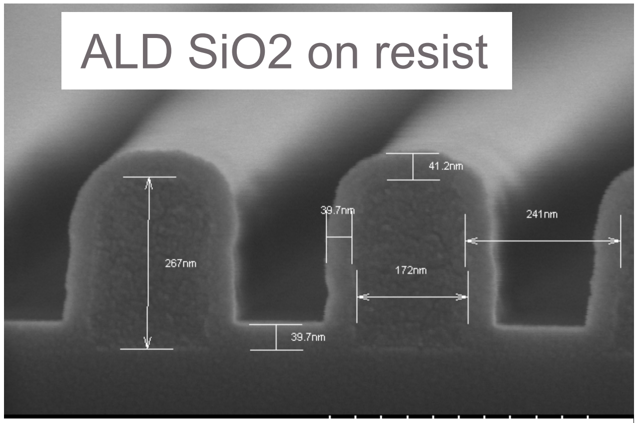
- High productivity single wafer tool for both PEALD and PECVD applications
- Accommodates up to 8 chambers by DCM
- PEALD and PECVD can be integrated on the same platform



DCM (Dual Chamber Module)

ALD ENABLING LITHOGRAPHY:
SPACER DEFINED DOUBLE/QUADRUPLE PATTERNING



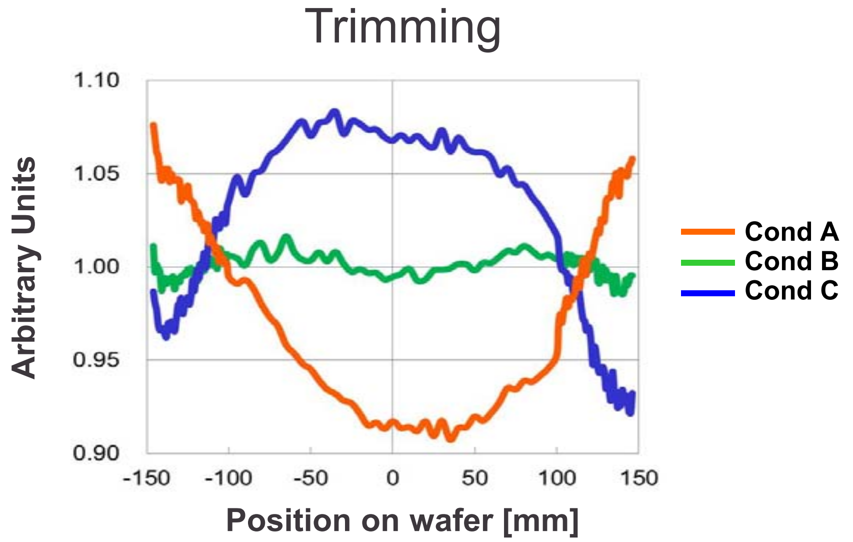


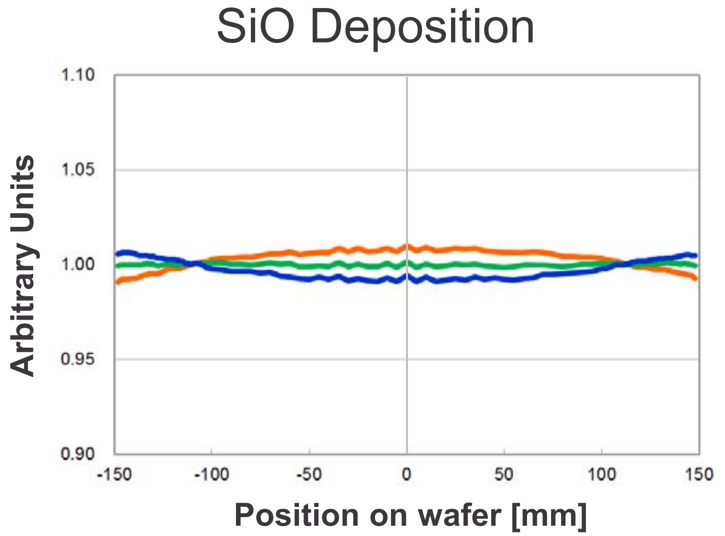
- ✓ **Spacer Defined Double Patterning (SDDP) with ALD in production since 3x nm DRAM and Flash**
- ✓ **Spacer Defined Quadruple Pattering (SDQP) in production for 1x nm Flash**
- ✓ **SDDP/SDQP qualified with 10nm Logic customers**

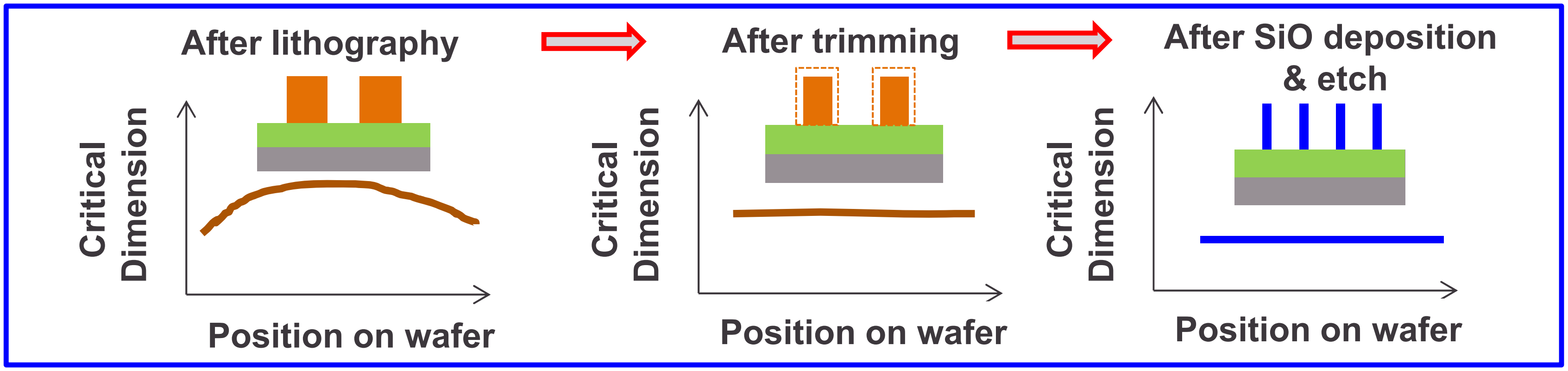
Key enablers brought by ALD

- Uniformity: CD control
- Low temperatures (<100C)
- Good step coverage
- Dense film
- In-situ trimming capability
- Extendible to other materials with etch selectivity

CD UNIFORMITY CONTROL



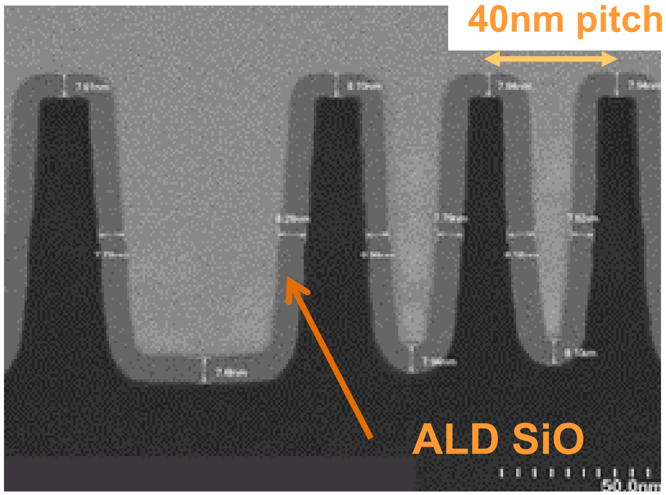


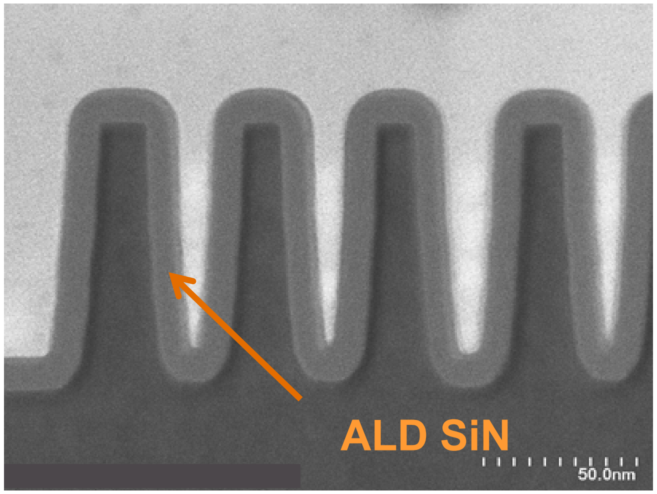


- WiW uniformity is controlled by trimming and deposition
- Trimming and deposition can mitigate the initial non-uniform resist pattern, which is to help within wafer CD uniformity

ALD SiO_2 and Si_3N_4 permanent spacers

- Low temperature (260 ~ 550 °C)
- Conformal
- High quality (low WER, low leakage current)



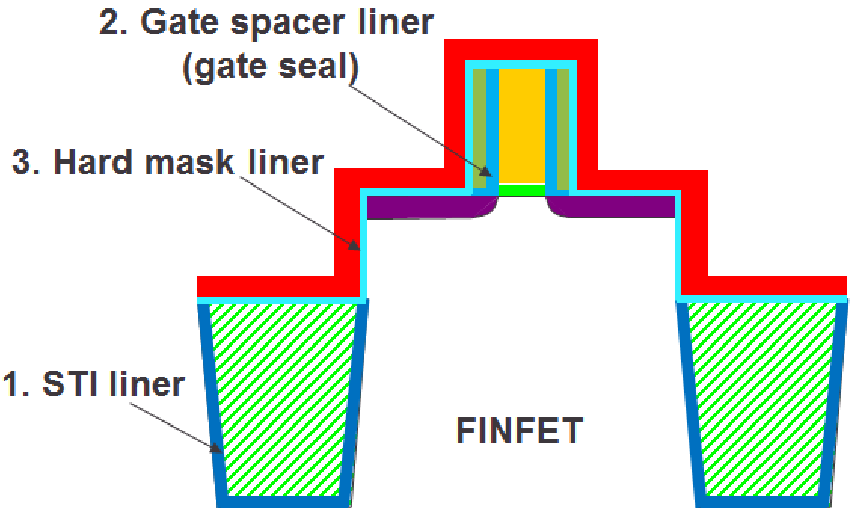


HIGH QUALITY SIO

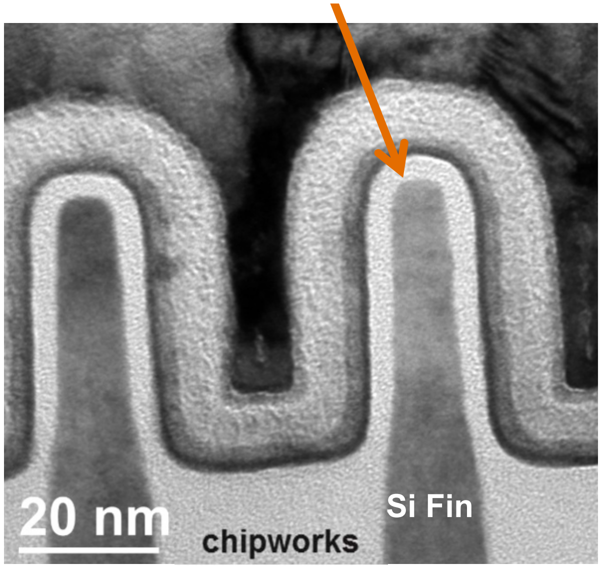
Single Wafer ALD

- Conformal thickness deposition is necessary for high-AR trench
- The film quality of the sidewall needs to be equal to that of top/blanket
- Deliver required electrical performance

Potential Applications:



IO gate SiO



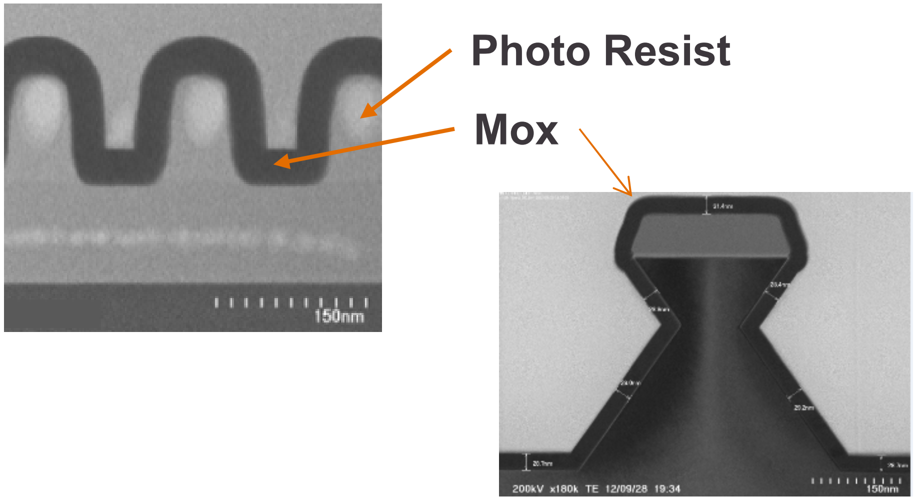
4. FinFET I/O Transistor Gate Oxide

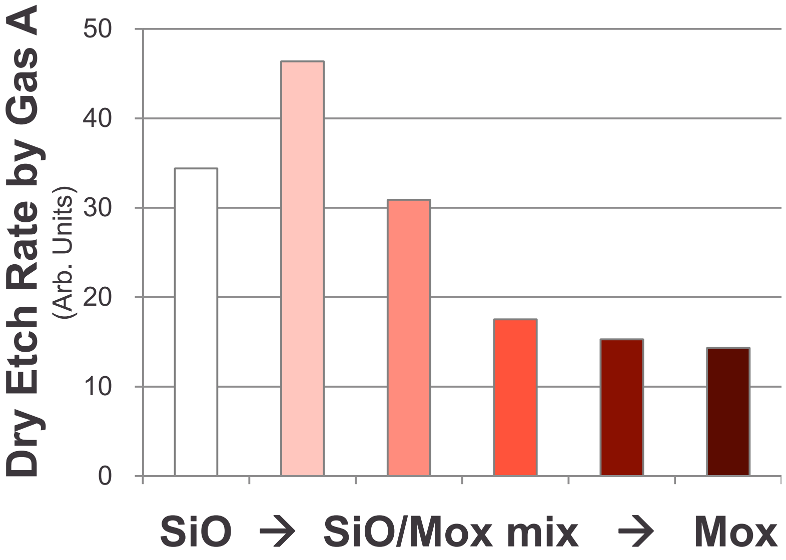
→ Development of High-temperature ALD SiO

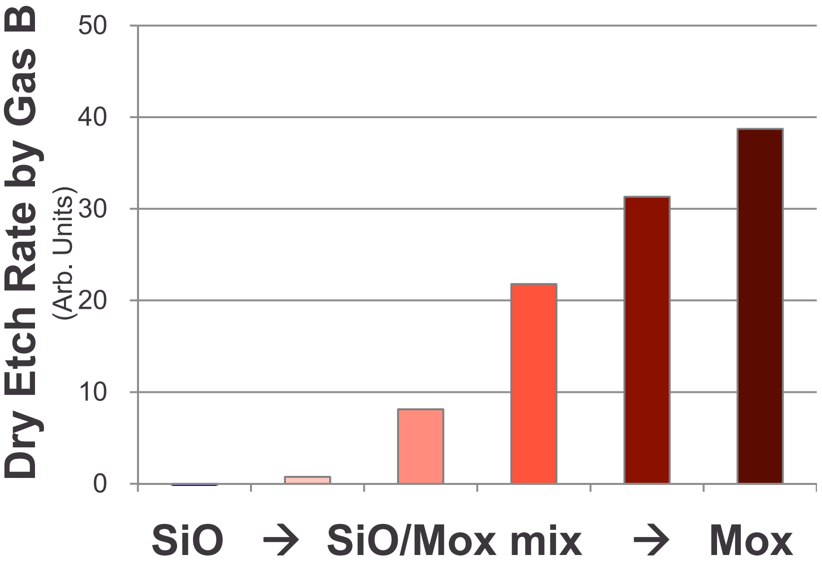
METAL OXIDE ADVANCED HARD MASK FOR PATTERNING

ALD Mox Etching Hard Mask

- Low/Tunable stress capable
- LT deposition: PR compatible
- Extension of etch selectivity portfolio



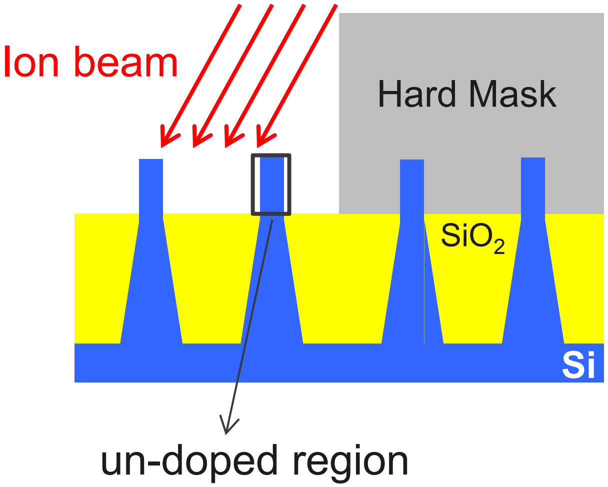




ADVANCED ALD DOPING

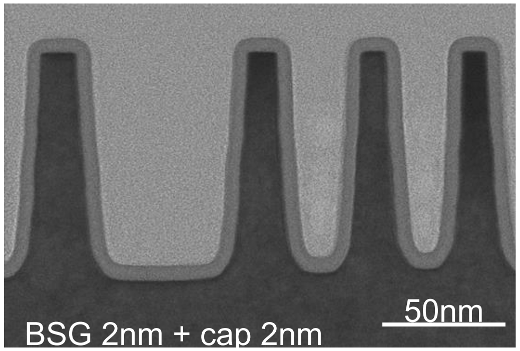
- ☐ FinFET requires conformal doping
- ☐ Limitations of conventional doping techniques like beam line:
  - Low conformality *(beam directionality, shadowing effect)*
  - Silicon damage

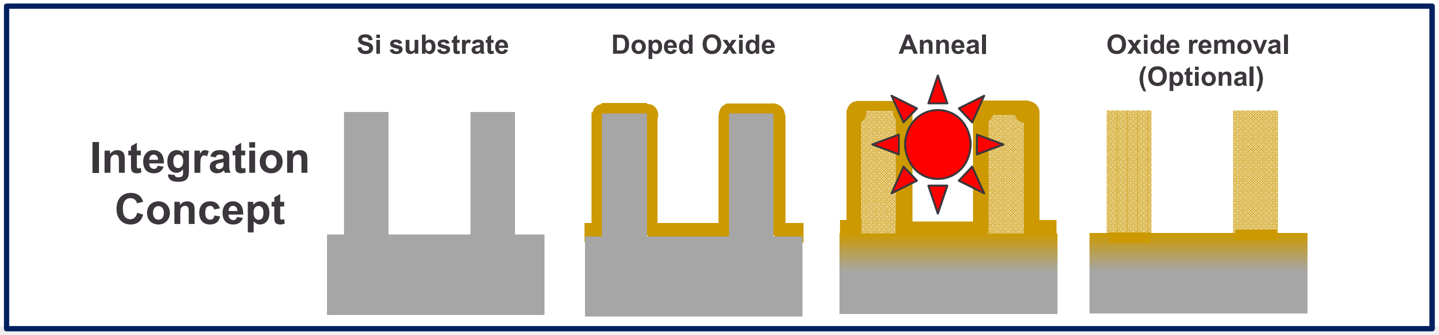
Shadowing effect



ALD Doping Benefits

Conformal & no silicon damage





ASM PRODUCTS
ADVANCED EPITAXY

Advanced transistors enabled with Intrepid® XP

- Relaxed & strained epitaxy for Si, SiGe & Ge based finFETs through 5nm
- Channel, Source/Drain stressor, contact & passivation cap layers

Integrated, low thermal budget pre-clean module

- High quality pre-Epi surface with low interface contamination

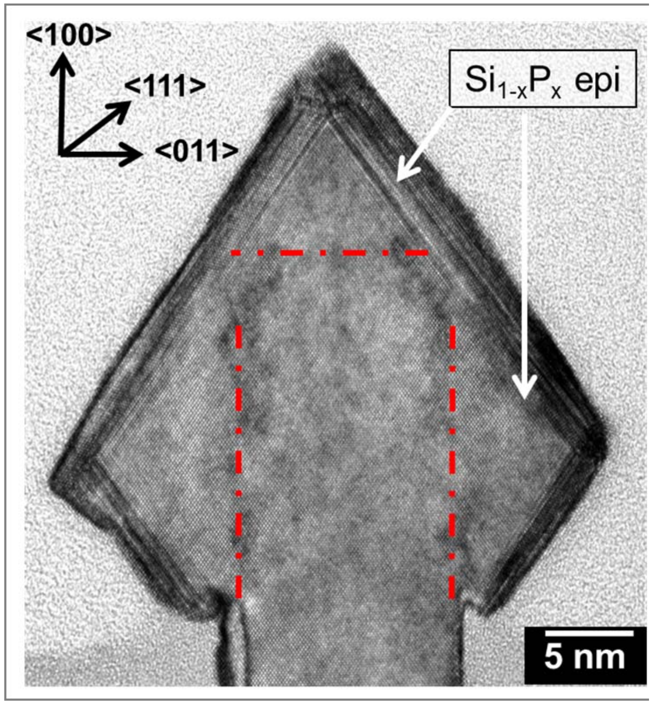
High productivity & lowest CoO

- XP Platform with up to 4 process modules
- Differentiated Epi film growth enabling devices with high drive currents & best-in-class productivity
- High throughput Epi processes with excellent uniformity, low defects & high doping levels

Intrepid® XP

EPI Si:P PROCESS

- **Epitaxial SiP film for nMOS finFETs**
- **Key Challenges**
  - Good Epi process selectivity
  - High P doping levels (>1E21 at/cm^2) for lower resistivity.
    - P concentration requirement increases at each node.
  - Thickness and dopant uniformity and repeatability
  - Low defects
  - Throughput, especially at lower temps
- **Integrated preclean required for pre-epi surface control**



J. Tolle, *et. al.*, ECS 2012.

EPI LAYERS FOR POWER DEVICES

- **Power devices require multiple & thick Epitaxial films to withstand high breakdown voltages (600V ~ 800V)**
- **Breakdown voltage of the device dictates number of Epi layers needed**
- **Doping level and uniformity of the Epi layers is critical and an ASM advantage**
- **In HVM at several power device manufacturers on 200 and 300mm**

ASM PRODUCTS
FURNACE CVD /DIFFUSION /BATCH ALD

A412 PLUS

- Dual boat/dual reactor system
- Clustering of different applications between reactors possible – only vertical furnace in the market with this capability
- Up to 150 product wafer load size
- Stocker design with integrated N2-FOUP purge and 36 FOUP positions

A400 for IoT and More than Moore

- Dual boat/dual reactor system

Applications:

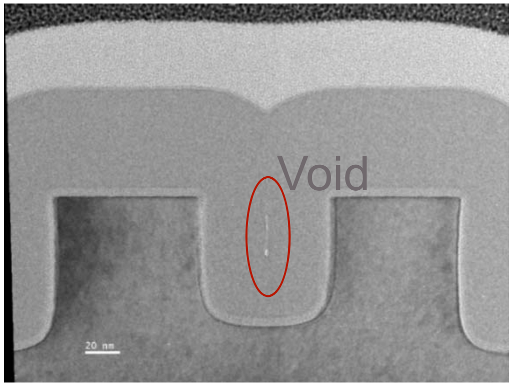
- Full range of applications for Logic, Memory, Power and MEMS

- LPCVD Silicon, SiN, TEOS, HTO
- Diffusion, Anneal, Cure, Reactive Cure
- Batch ALD (AlO, AlN, TiN, SiN, SiO, etc)

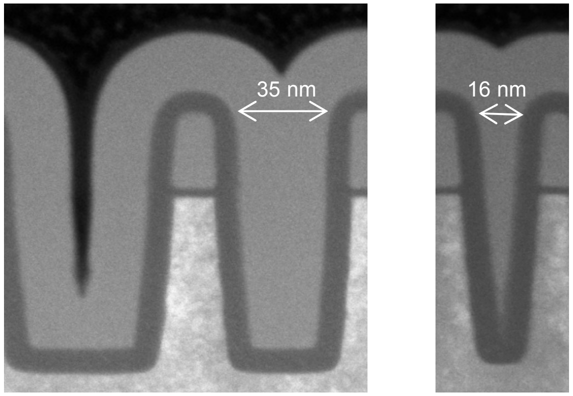
A400/A412 FURNACE - INNOVATION

Example 1: Voidless silicon gapfill.

- Voidless gapfill of rectangular trenches is a challenge for technologies beyond 10nm
- Standard silicon gap fill:

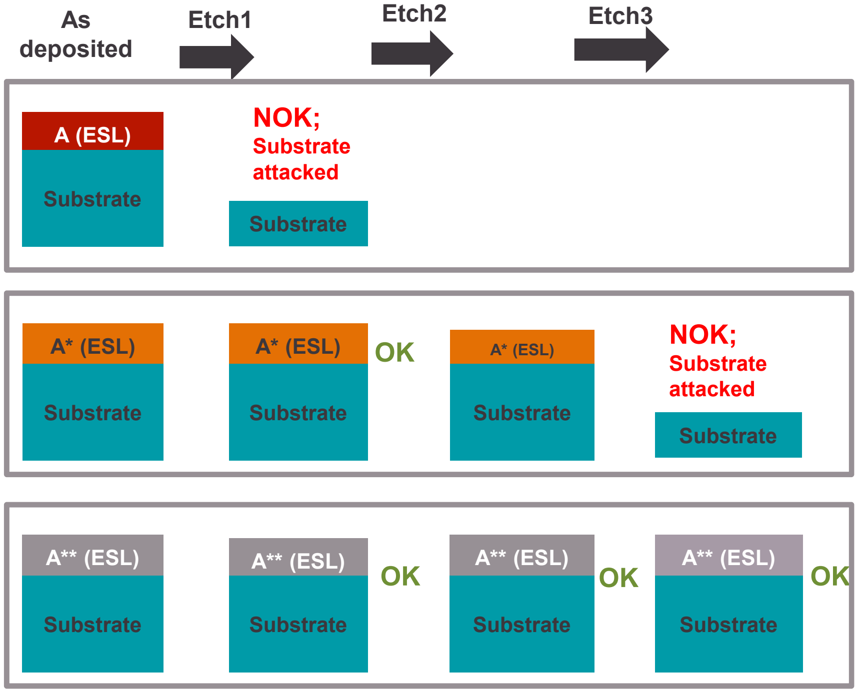


- ASM solution. Voidless gap fill even for narrow widths, with high throughput:



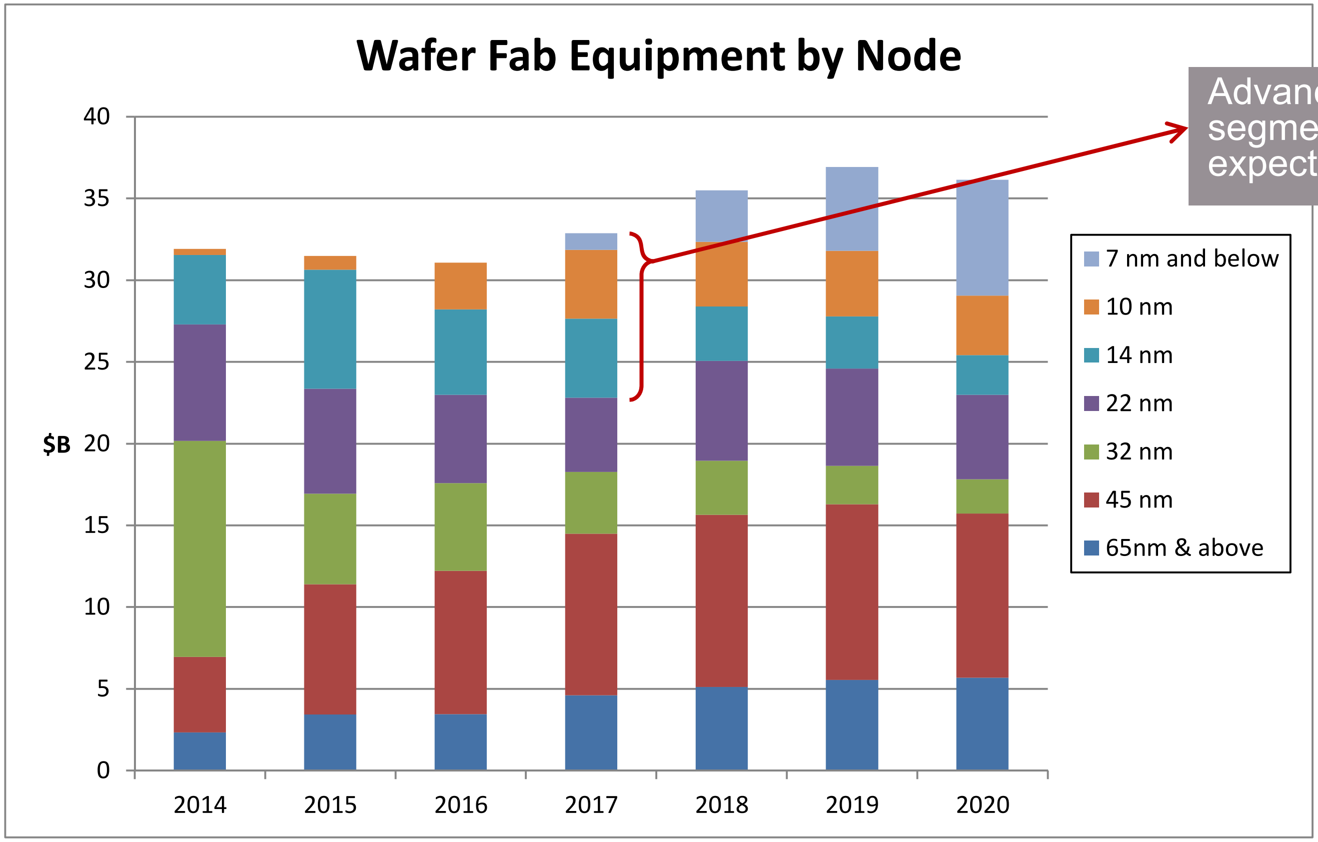
Example 2: Etch stop layers (ESL)

- Future nodes with complex patterning require advanced ESL with high etch selectivity towards Si, SiO and SiN
- ESL (A** in figure below) was developed that protects substrate even for complex schemes:



As deposited	Etch1	Etch2	Etch3
A (ESL) Substrate	NOK; Substrate attacked Substrate		
A* (ESL) Substrate	A* (ESL) Substrate OK	A* (ESL) Substrate	NOK; Substrate attacked Substrate
A** (ESL) Substrate	A** (ESL) Substrate OK	A** (ESL) Substrate OK	A** (ESL) Substrate OK

WAFER FAB EQUIPMENT FORECAST



Advanced nodes: market segments with high expected growth

Gartner July, 2016

Key customer ALD penetrations in advanced nodes: market segments with high expected growth

OUTLINE

- **Exponentials in the industry**
- **New Materials and 3D: Moore's law enablers**
- **ASM and New Materials**
  - ALD as enabler of new materials
  - ASM New Materials development strategy
  - ALD supply chain components
- **ASM Products and selected applications**
- **Summary and Conclusions**

SUMMARY AND CONCLUSIONS

- Scaling is increasingly enabled by new materials and 3D technologies
- ALD enables new materials and 3D
- Hafnium based ALD high-k gates on ASM Pulsar® extendable for 4 device generations
- ALD patterning films portfolio extended with metal oxide hardmasks
- ALD Doped oxides solution for fin doping
- High quality liners, spacers enabled by ALD
- Intrepid® XP, system with up to 4 Epi reactors, targeting strained Epi layers for CMOS, and Epsilon® 3200 for analog/power
- ASM's Vertical Furnace is providing high productivity, in combination with continued process innovation

ASM

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